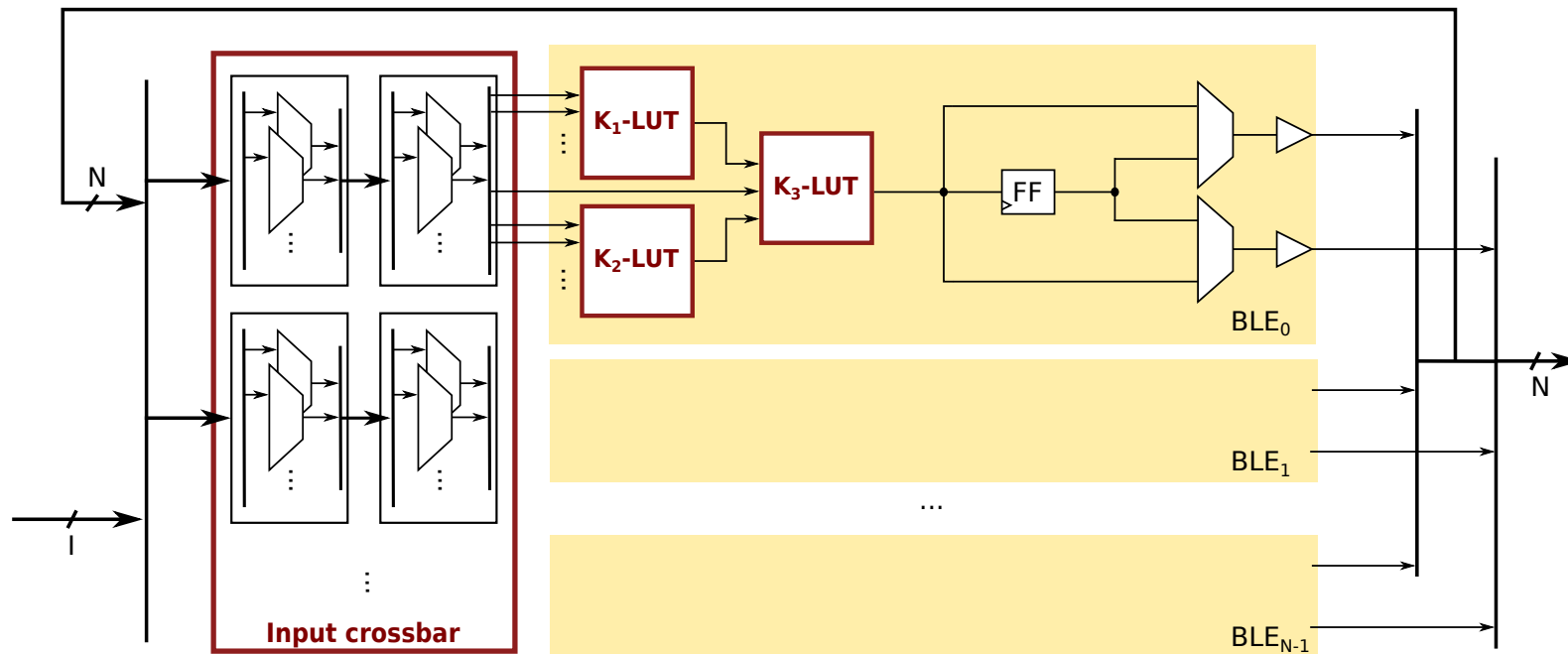


FPRESSO

Enabling Express Transistor-Level Exploration of FPGA Architectures

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Architecture Exploration



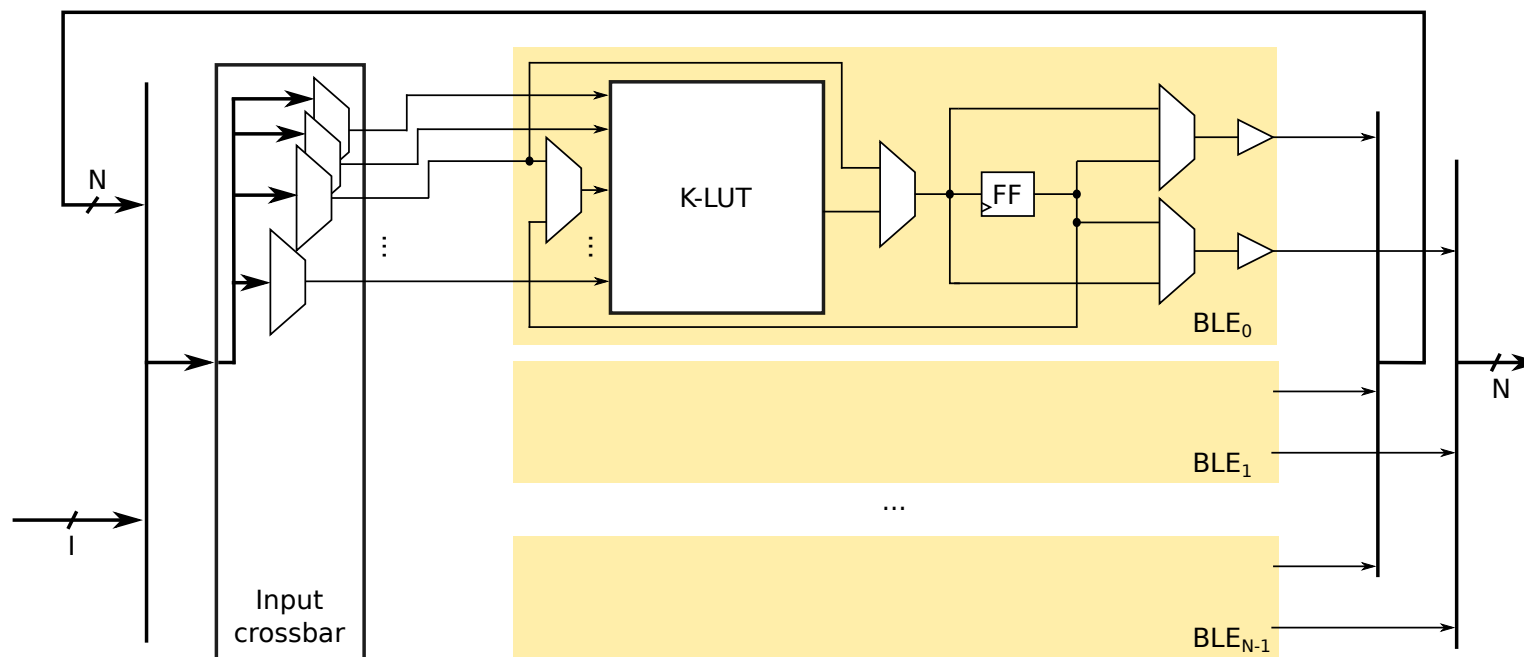
Existing Tool: COFFE

Pros

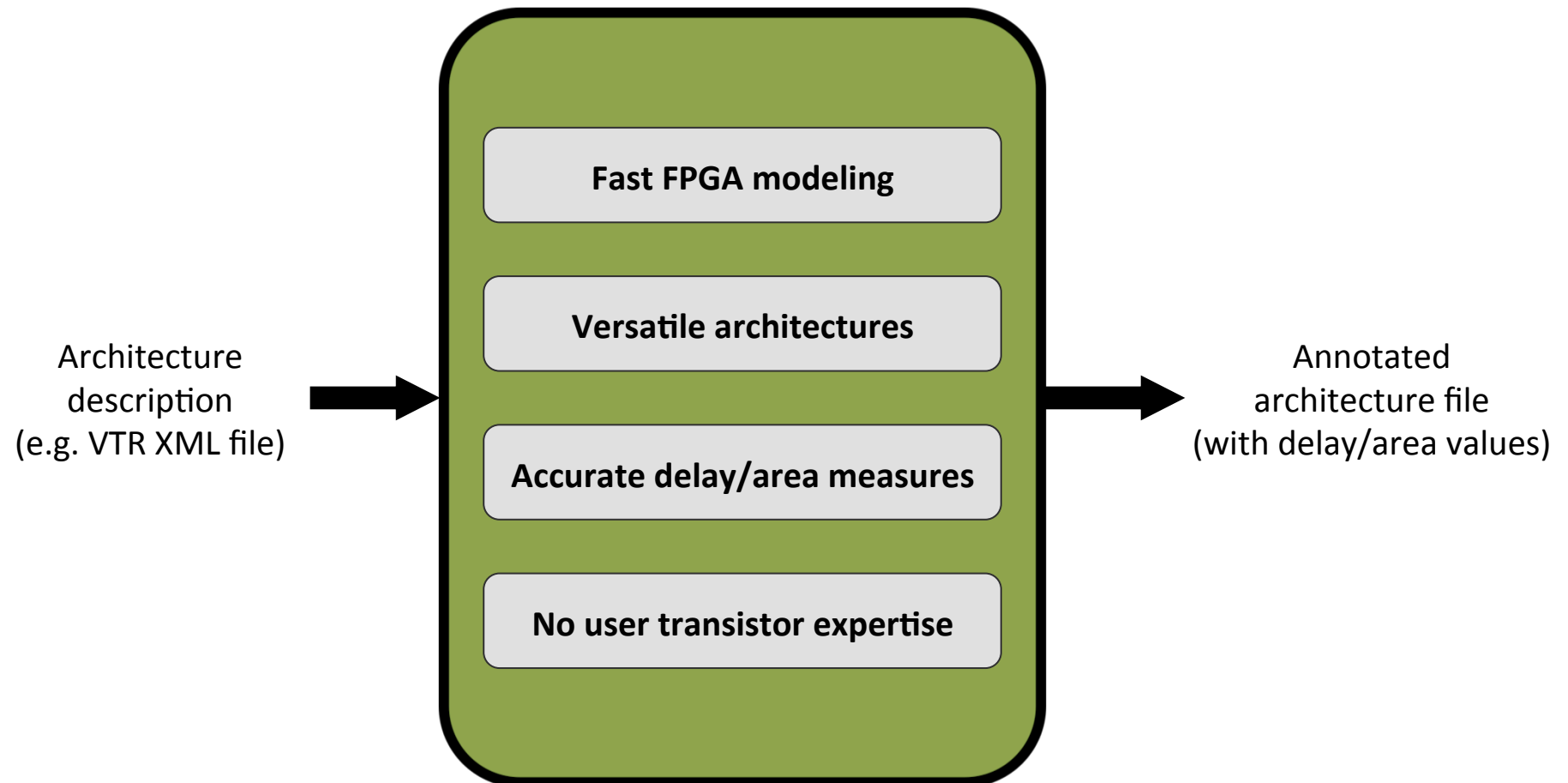
- Parameterizable architecture
- Accurate delay/area measures

Cons

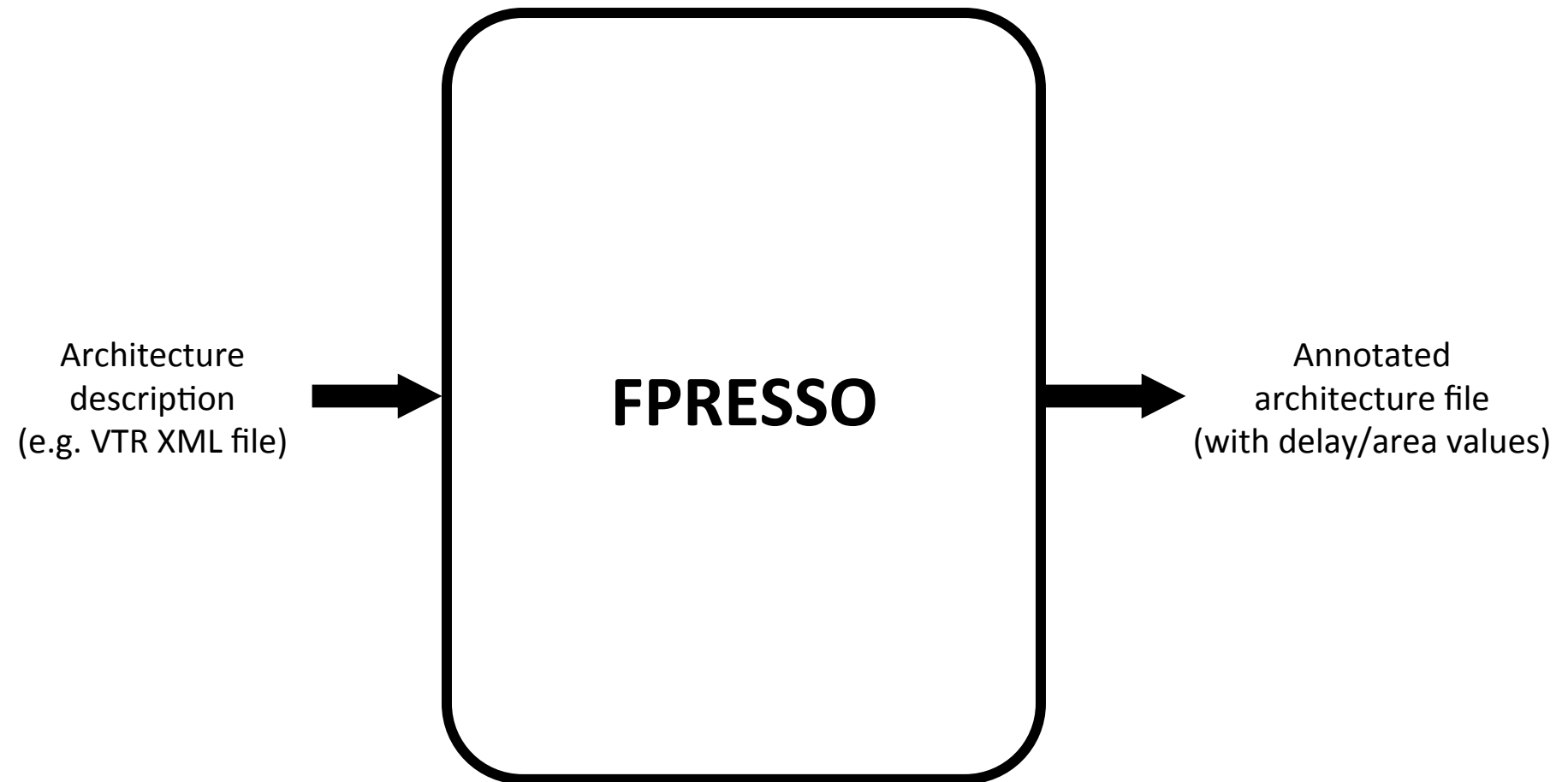
- Fixed structure
- Slow (several hours)



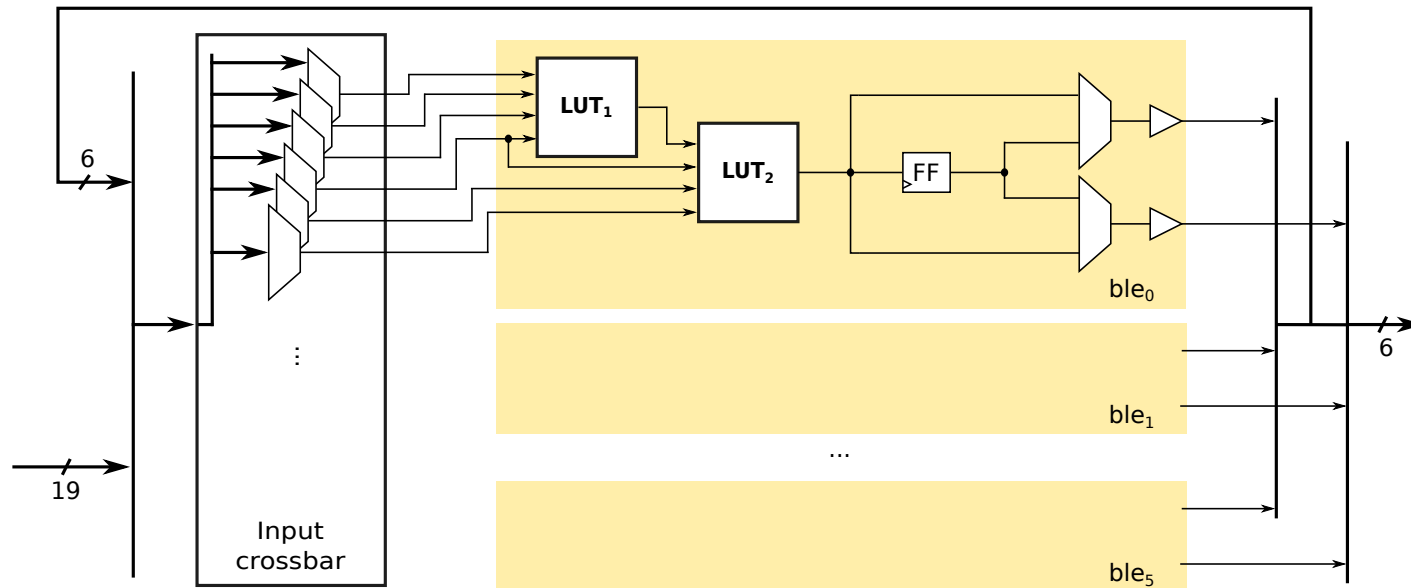
Objective



Objective



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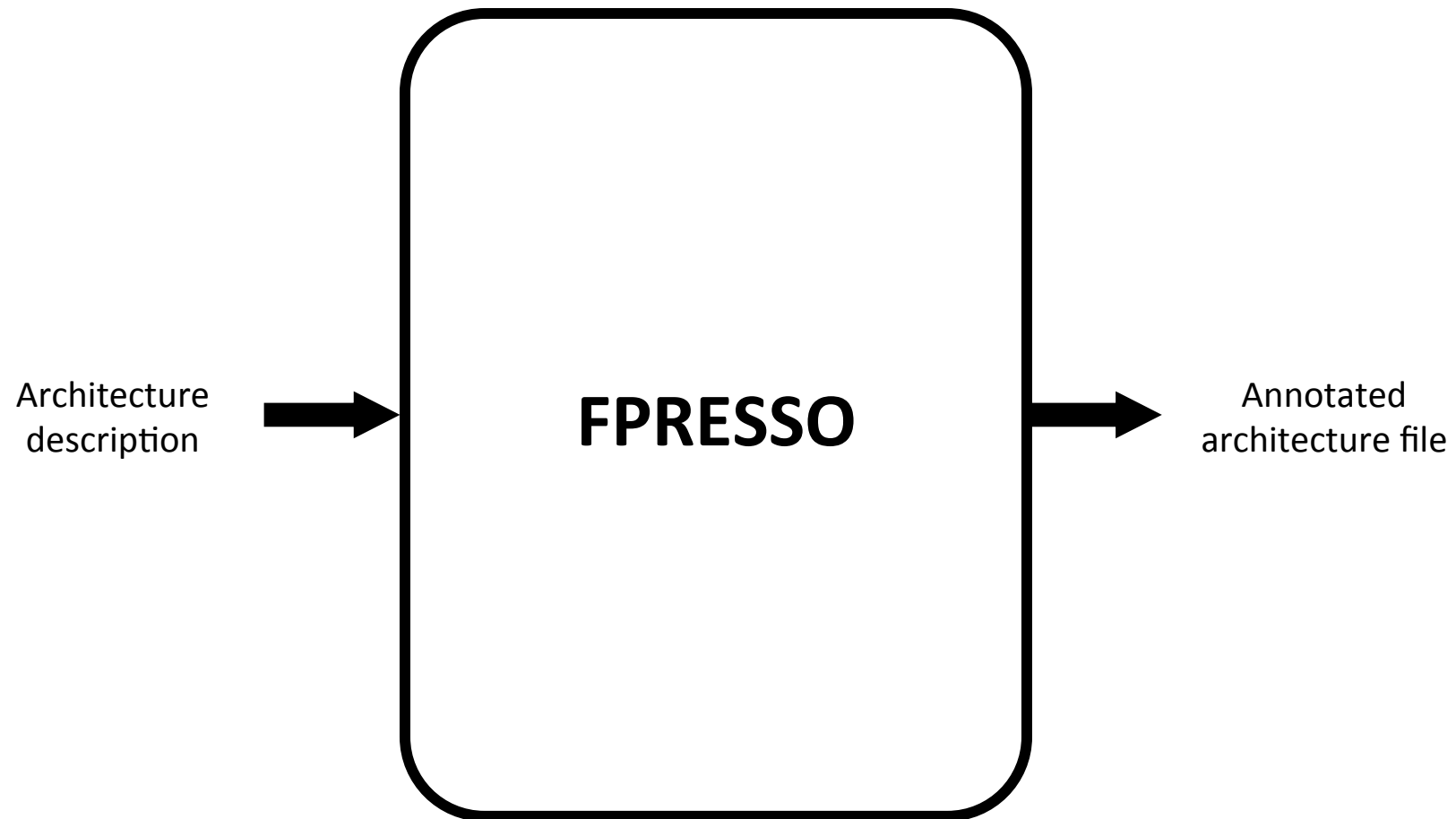


```

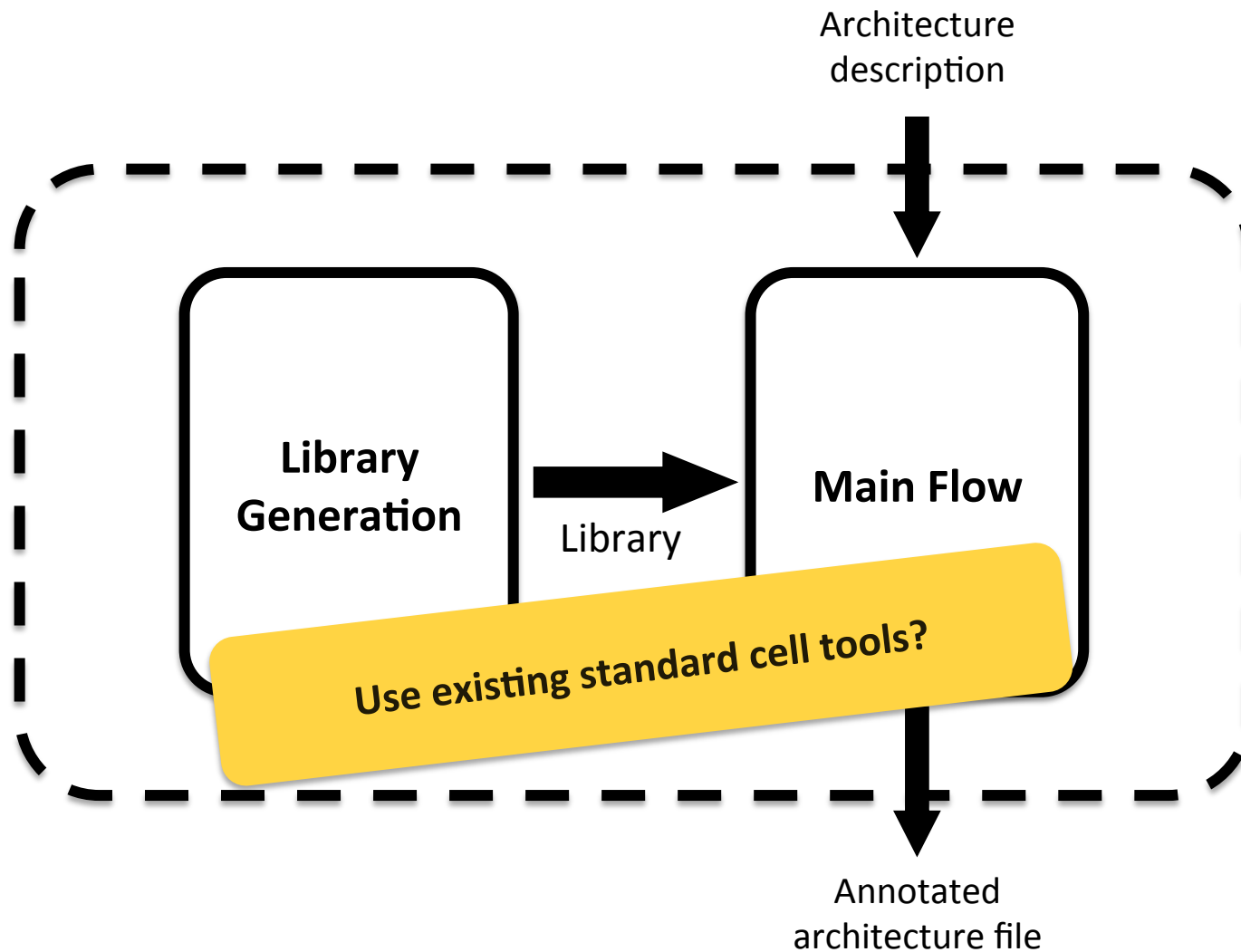
<pb_type name="clb" num_pb="1" num_in="19" num_out="6">
  <pb_type name="ble" num_pb="6" num_in="6" num_out="2">
    <pb_type name="lut1" num_pb="1" num_in="4" num_out="1"/>
    <pb_type name="lut2" num_pb="1" num_in="4" num_out="1"/>
    <pb_type name="ff" num_pb="1" num_in="1" num_out="1" clock="clk"/>
    <mux name="combseqfdb" input="ff.Q lut2.out" output="ble.out[0]"/>
    <mux name="combseqout" input="ff.Q lut2.out" output="ble.out[1]"/>
    <direct name="lutinA" input="ble.in[3:0]" output="lut1.in"/>
    <direct name="lutinB" input="ble.in[5:3]" output="lut2.in[3:1]"/>
    <direct name="lutinC" input="lut1.out" output="lut2.in[0]"/>
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  <crossbar type="complete" name="inputxbar" input="clb.in ble.out[0]" output="ble.in"/>
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</pb_type>

```

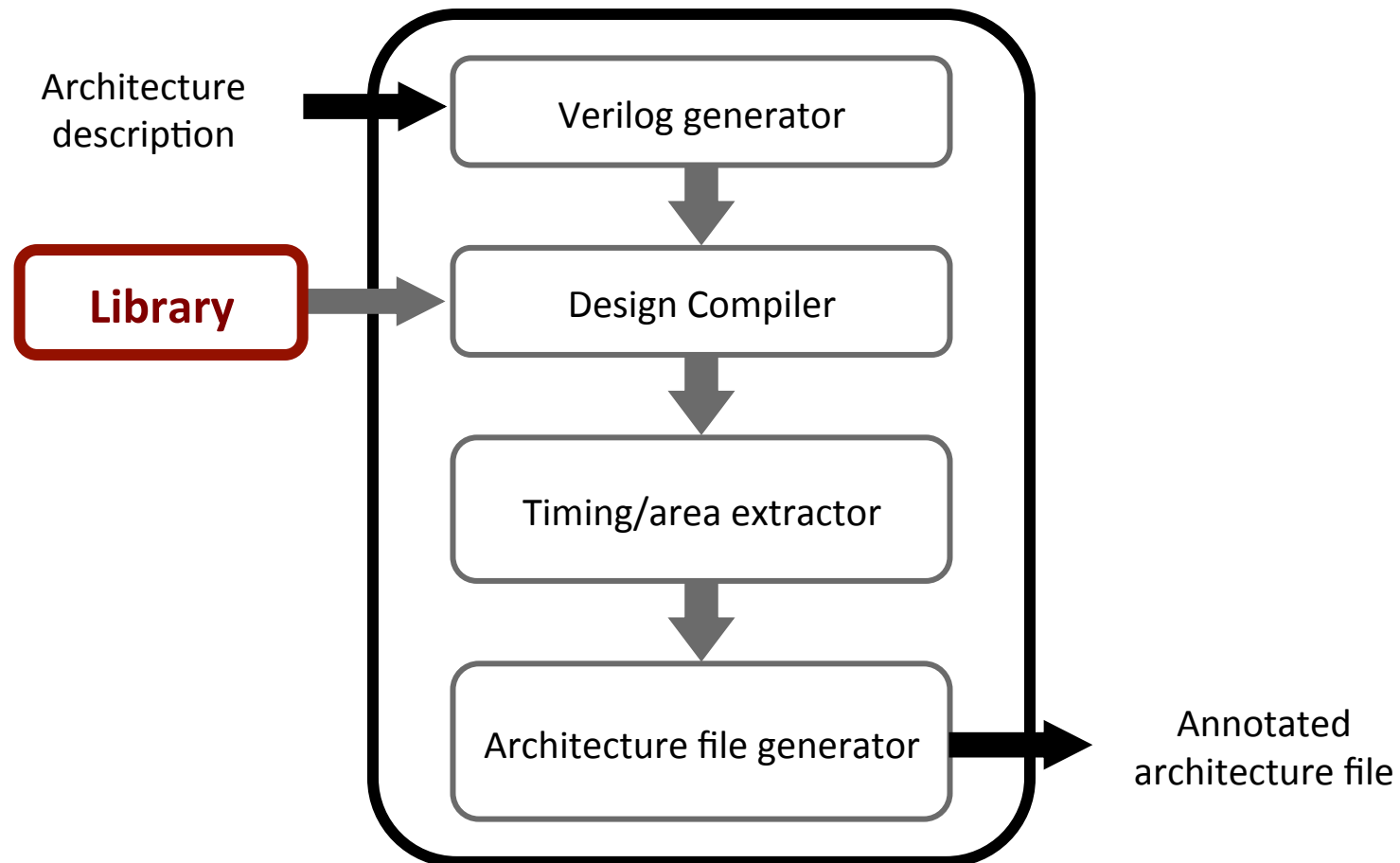
Interface



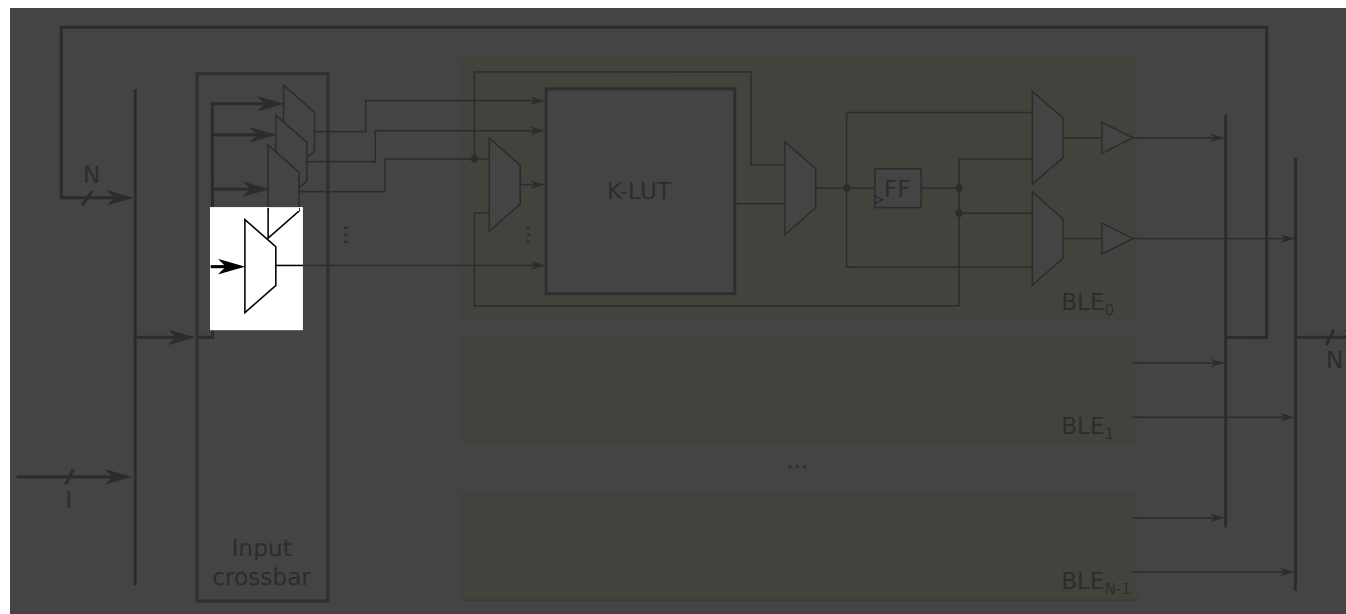
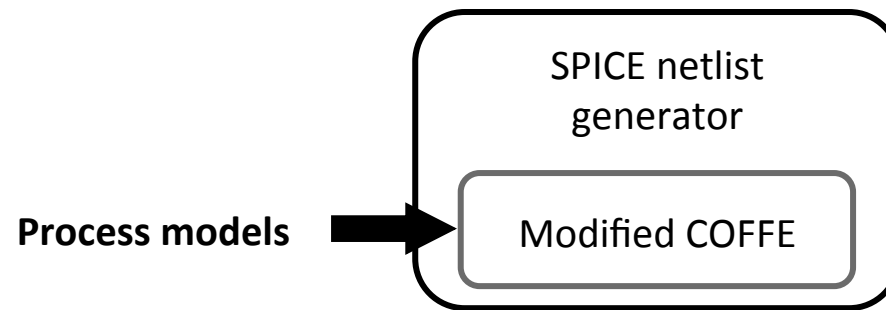
Complete Flow



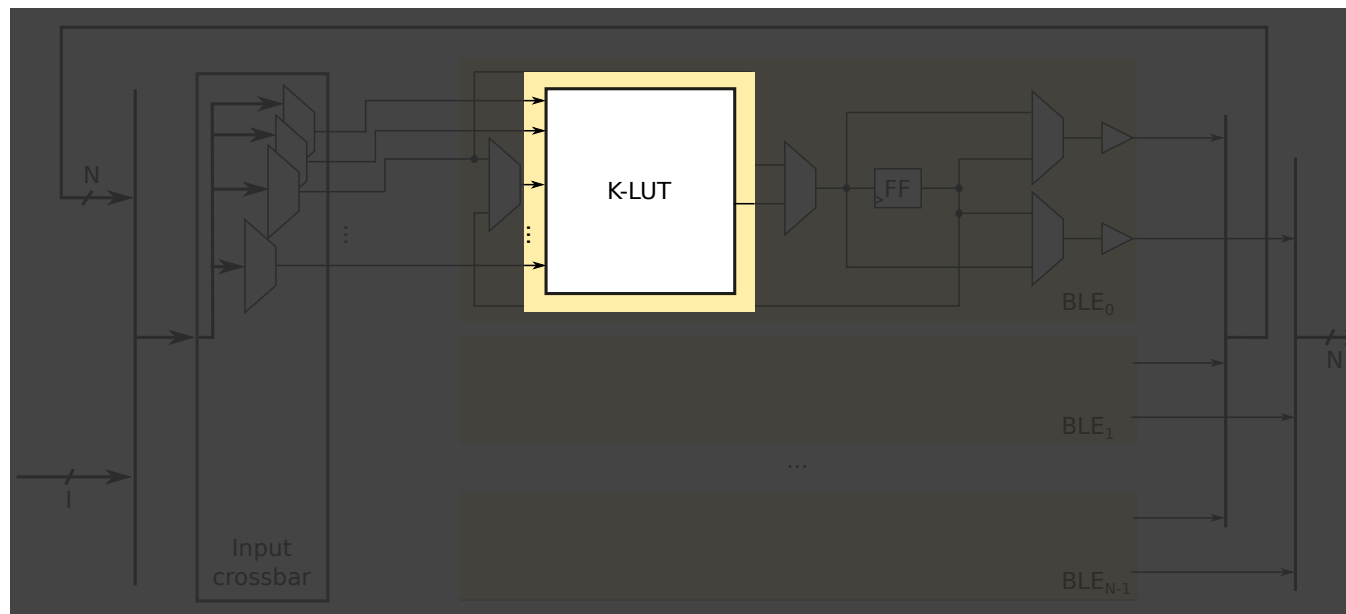
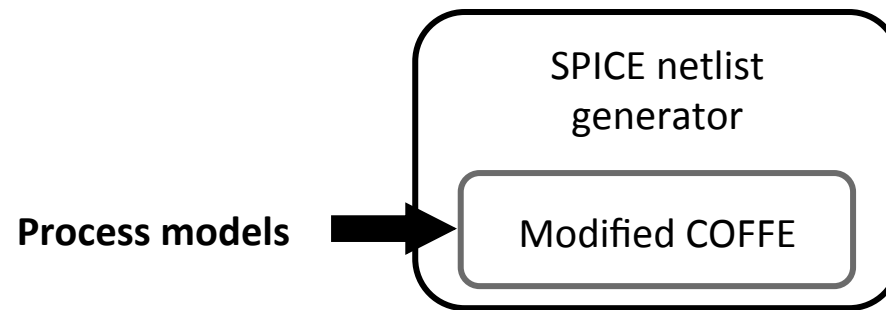
Main Flow



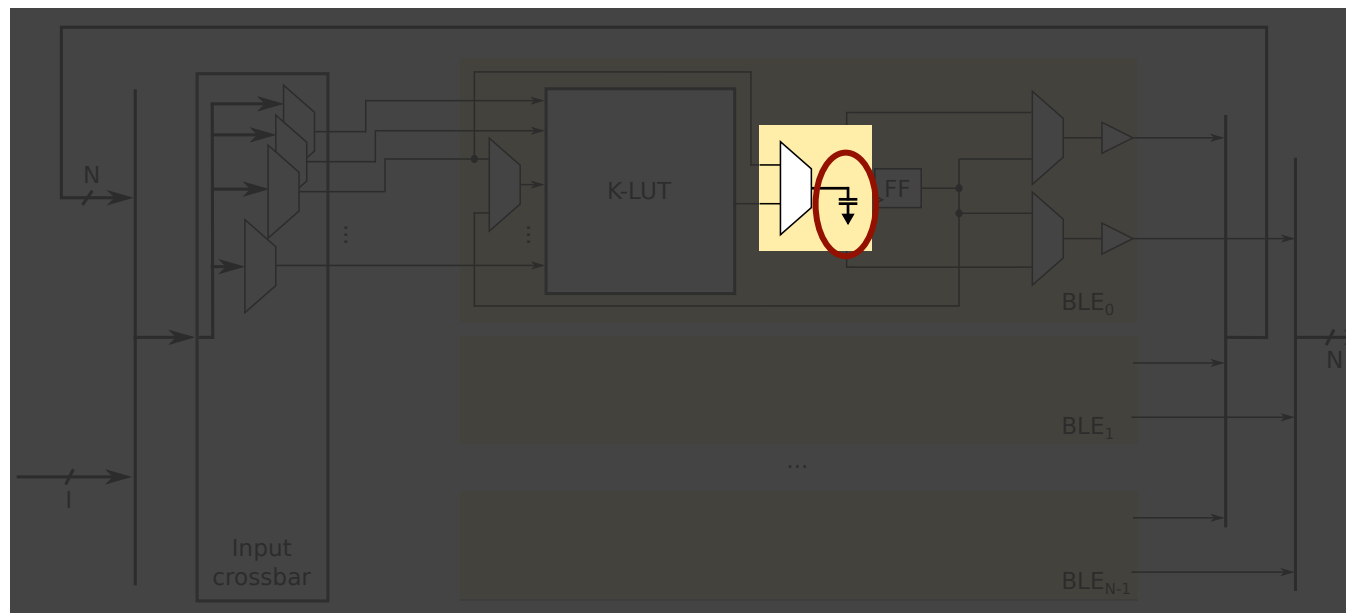
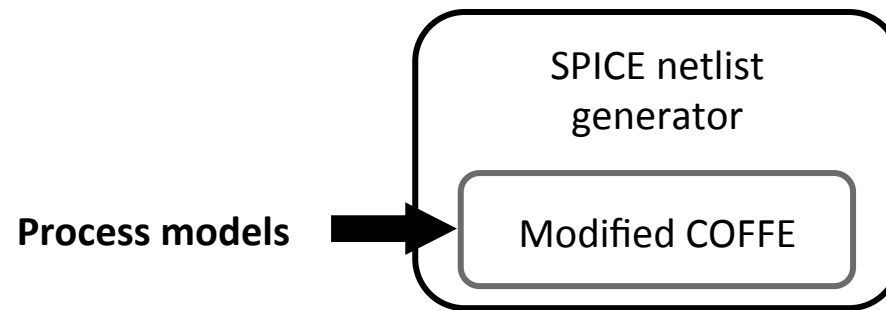
Library Generation



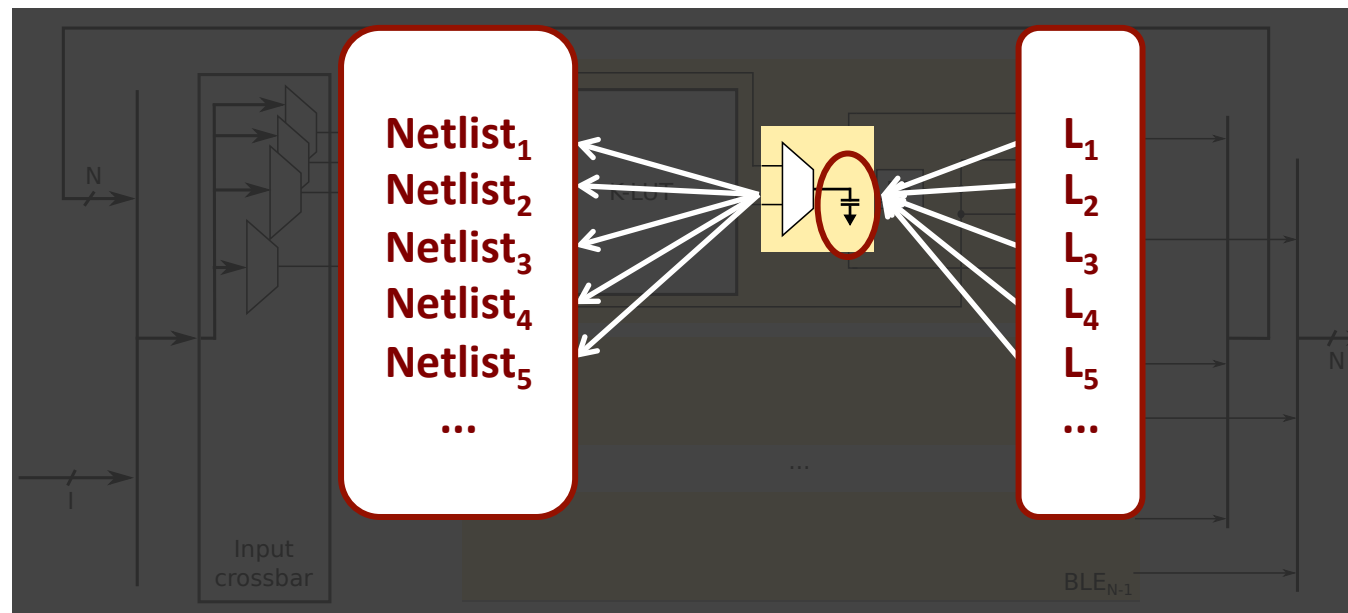
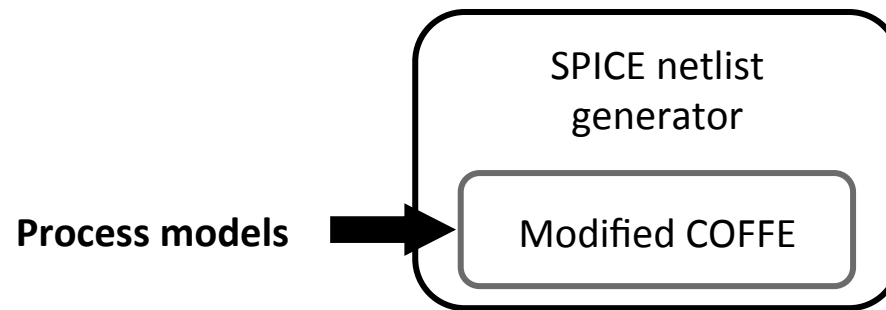
Library Generation



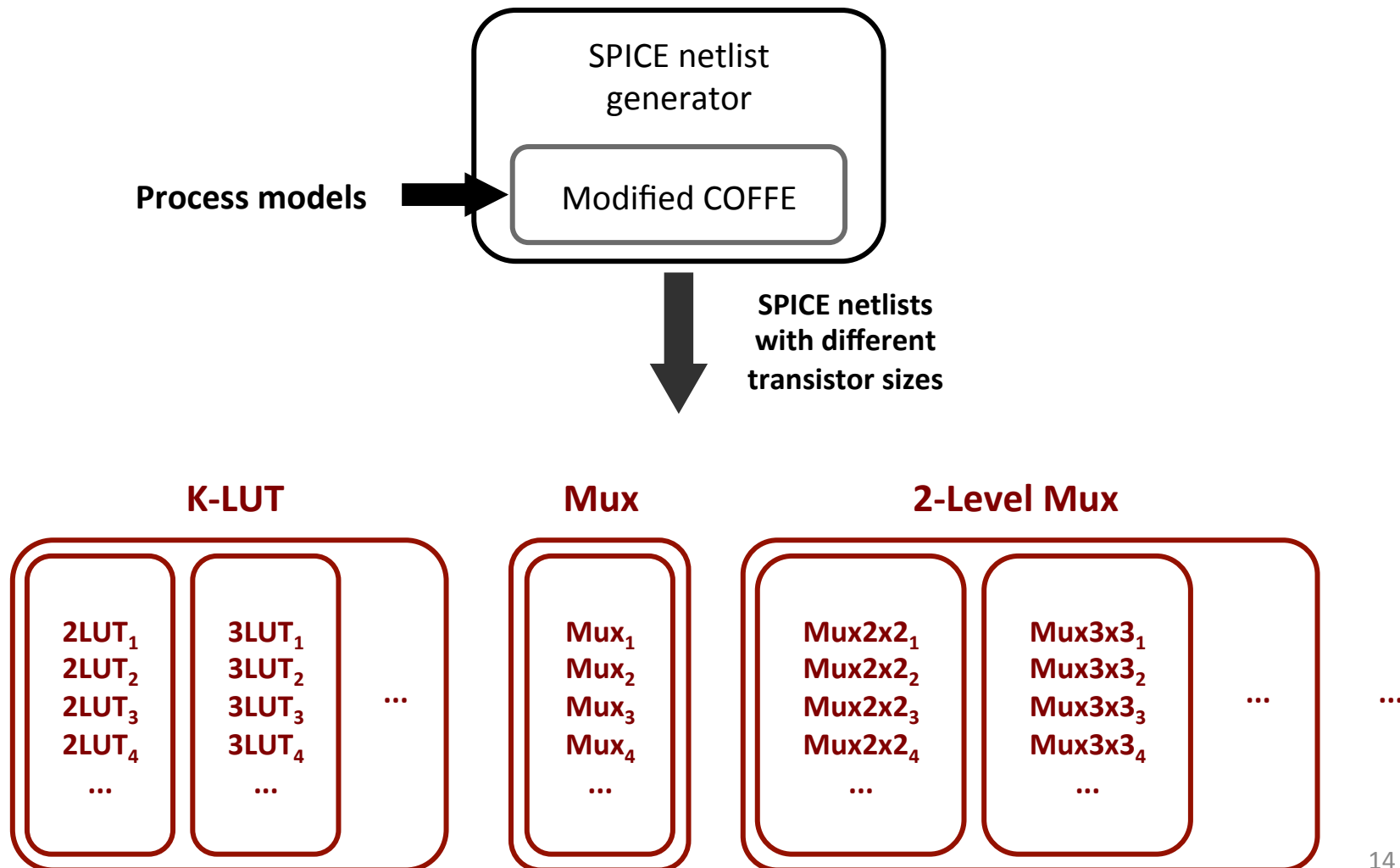
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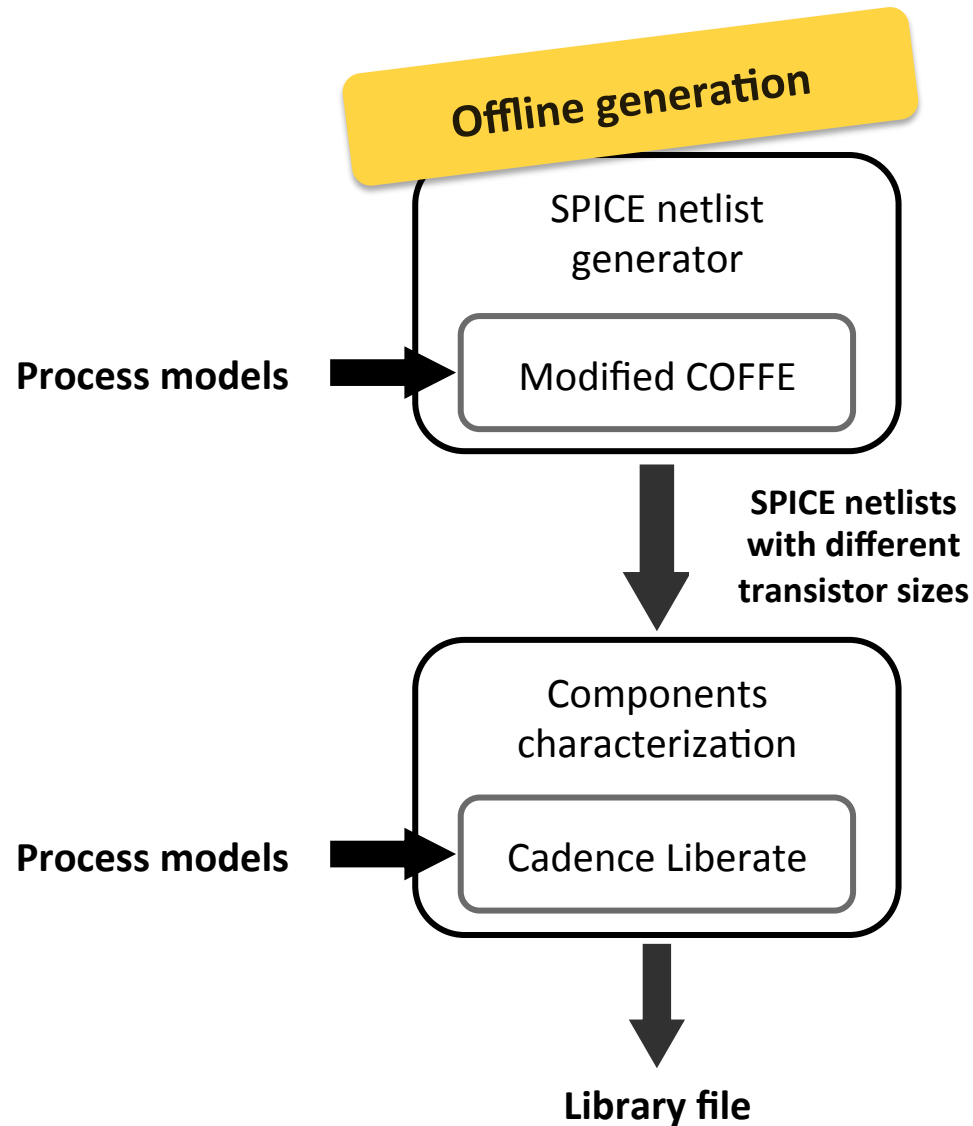
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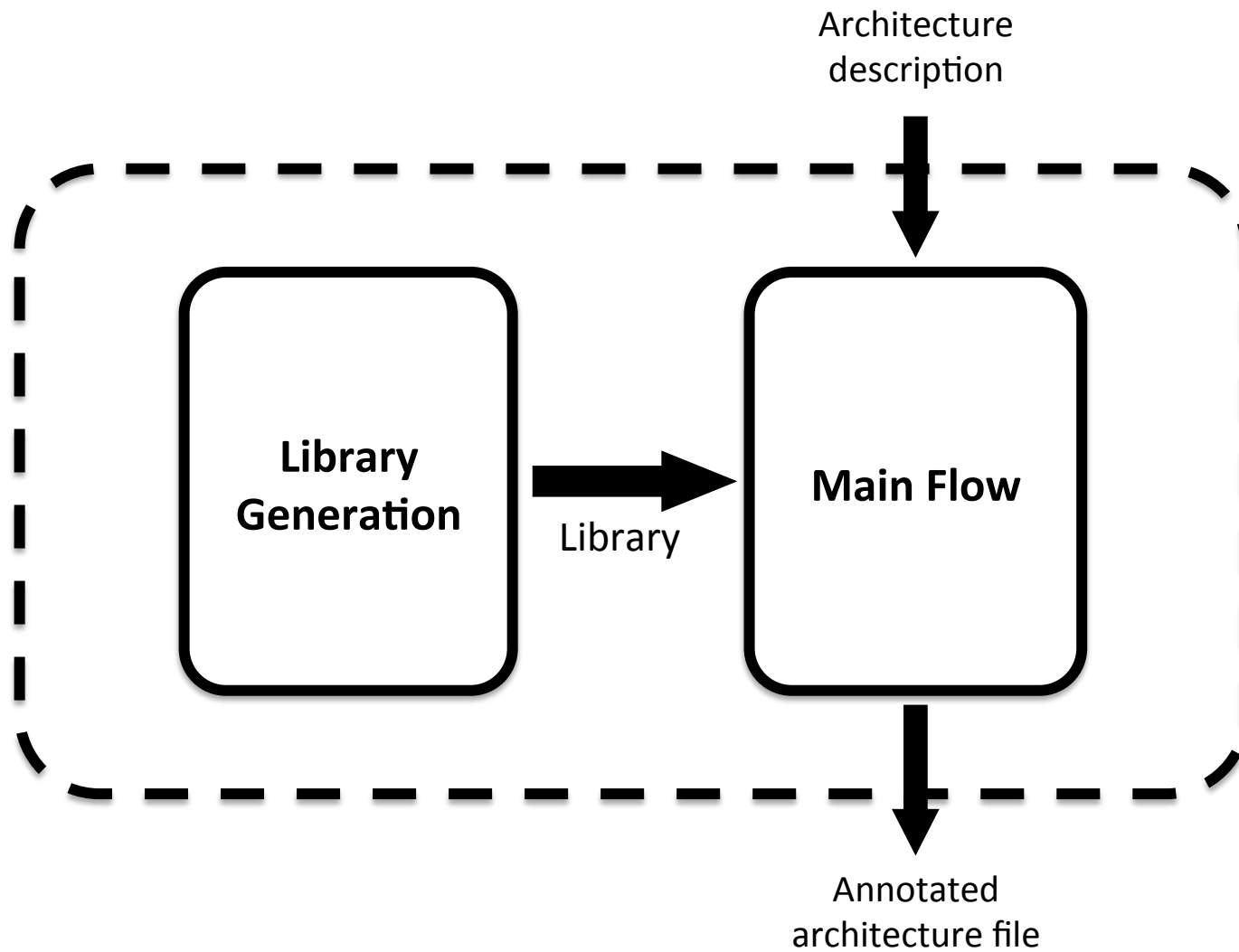
Library Generation



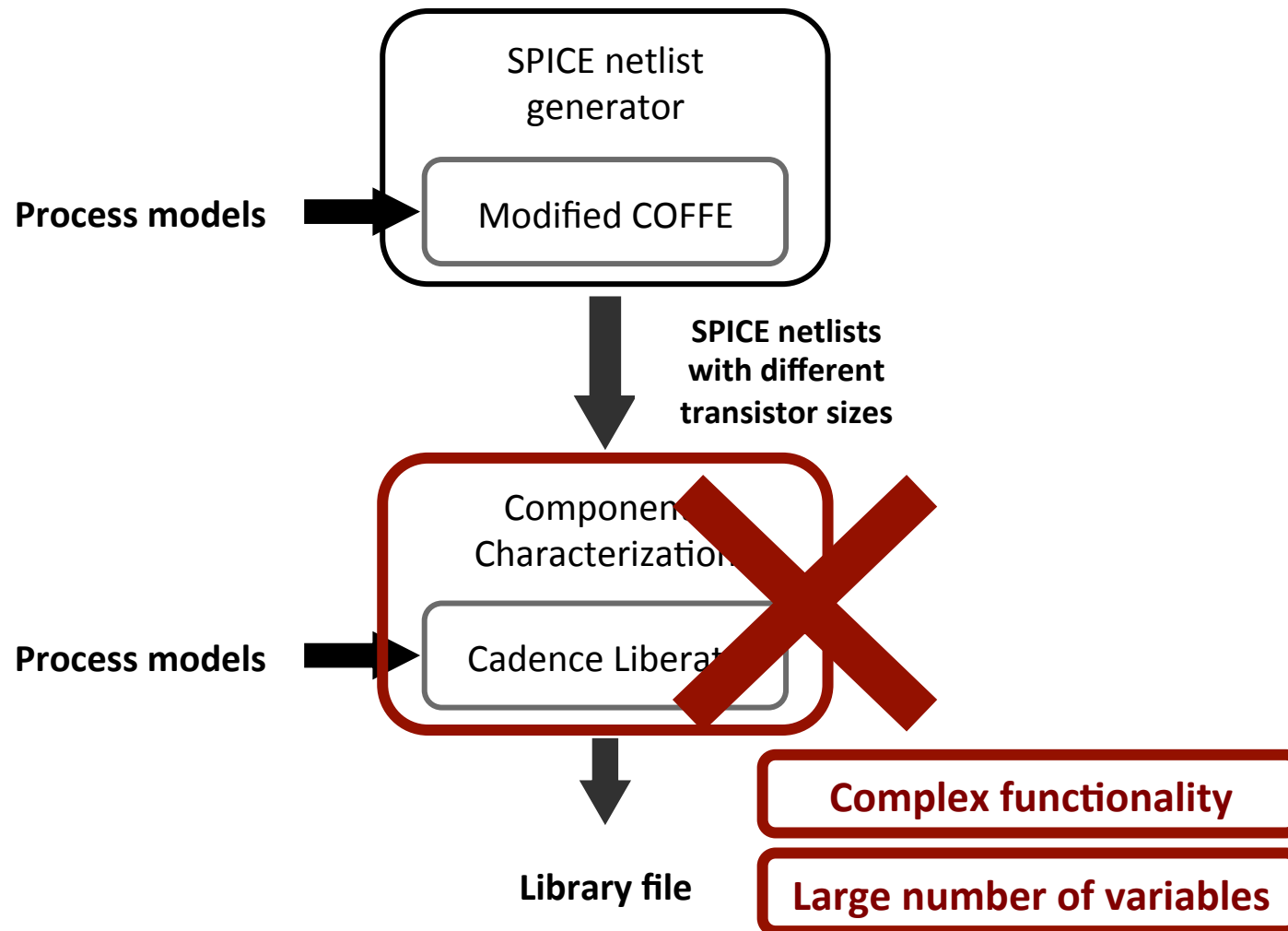
Library Generation



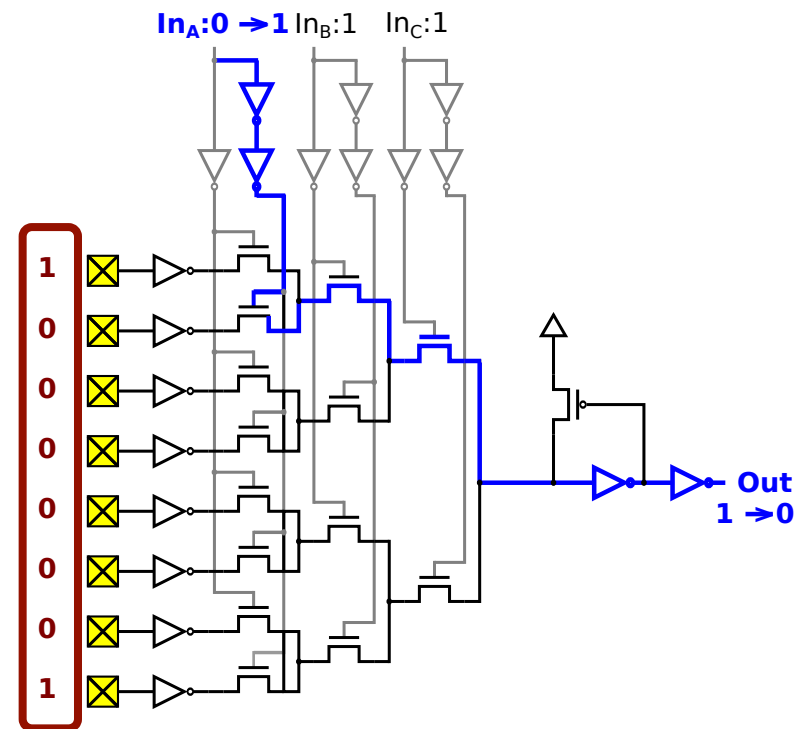
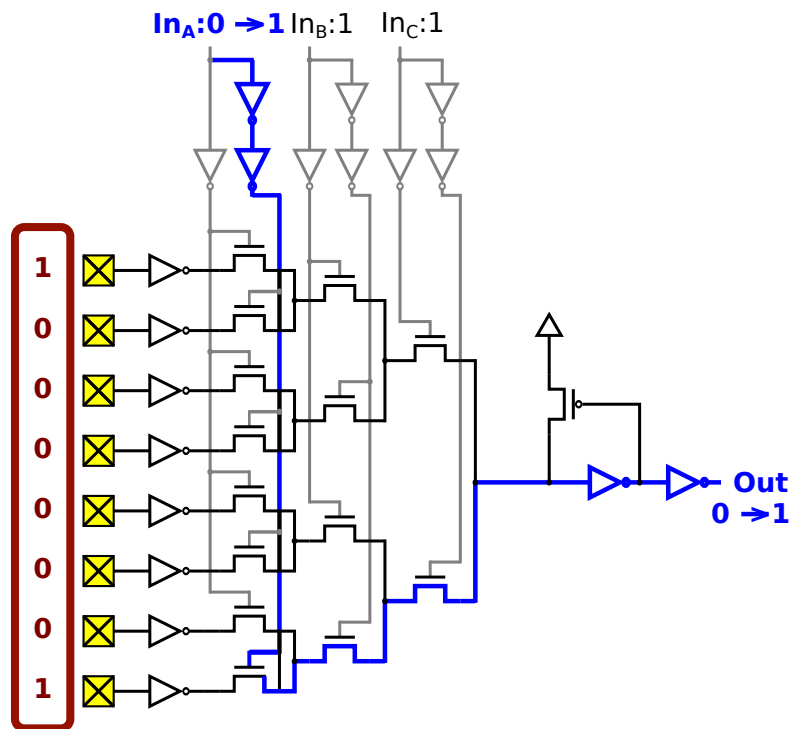
Complete Flow



Library Generation



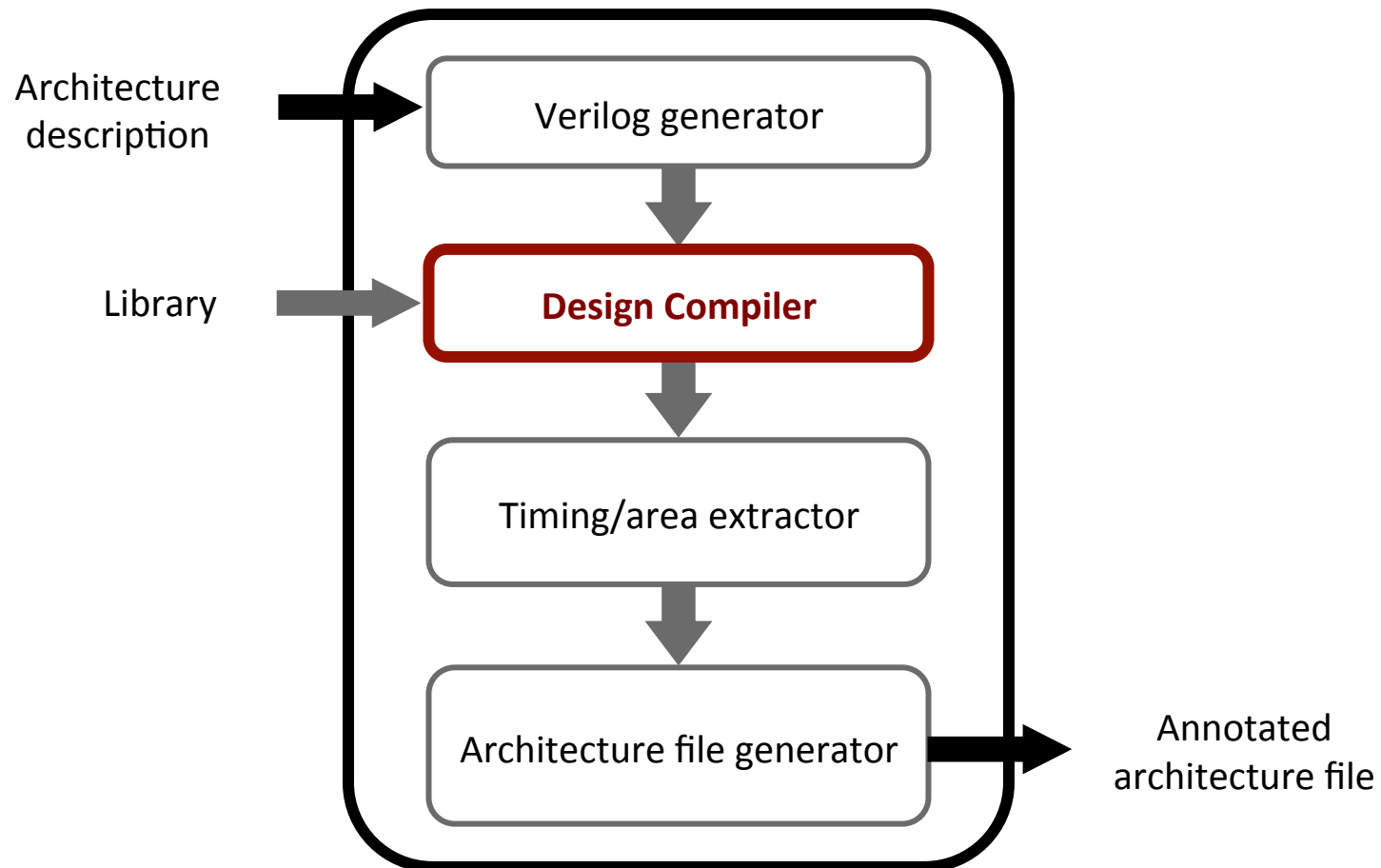
LUT Characterization



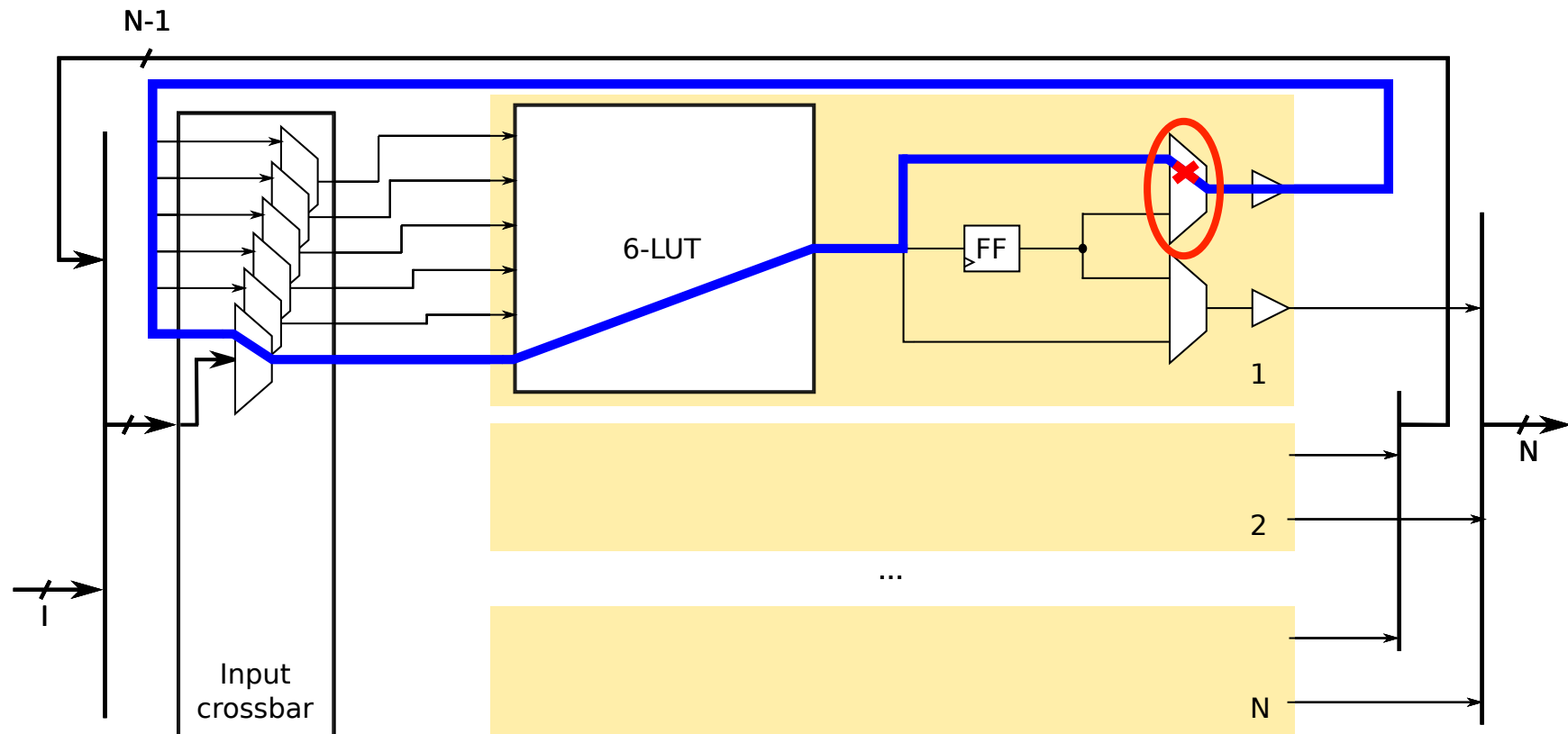
3-LUT \rightarrow 11 variables \checkmark

6-LUT \rightarrow 70 variables \times

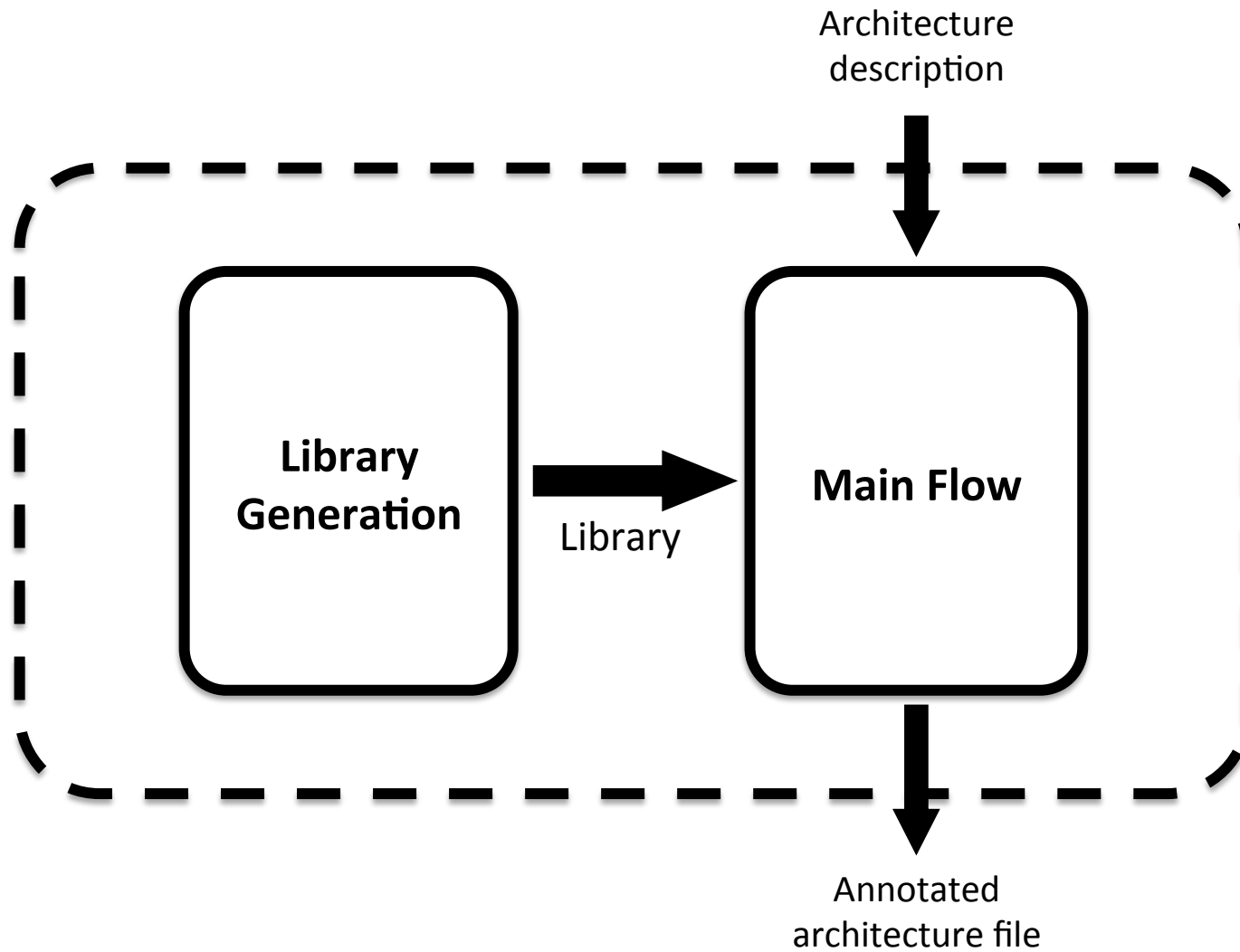
Main Flow



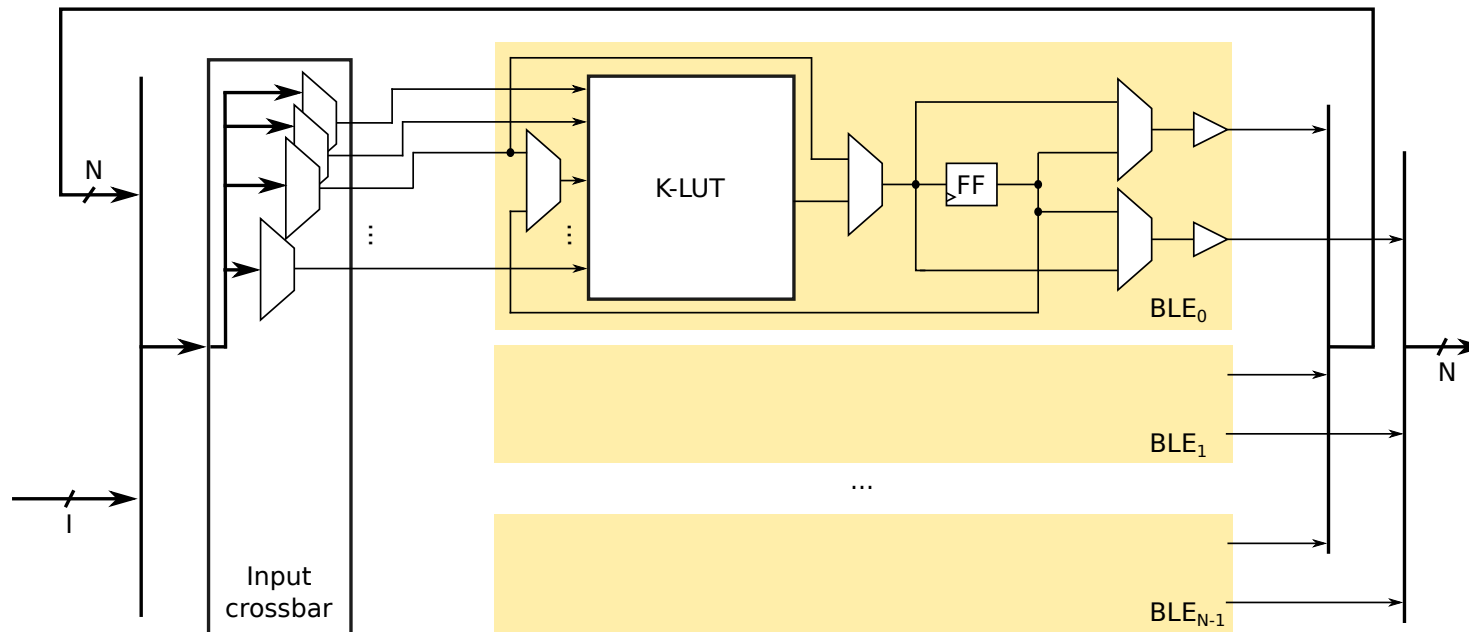
Combinational Loops



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FPRESSO vs. COFFE



Parameters

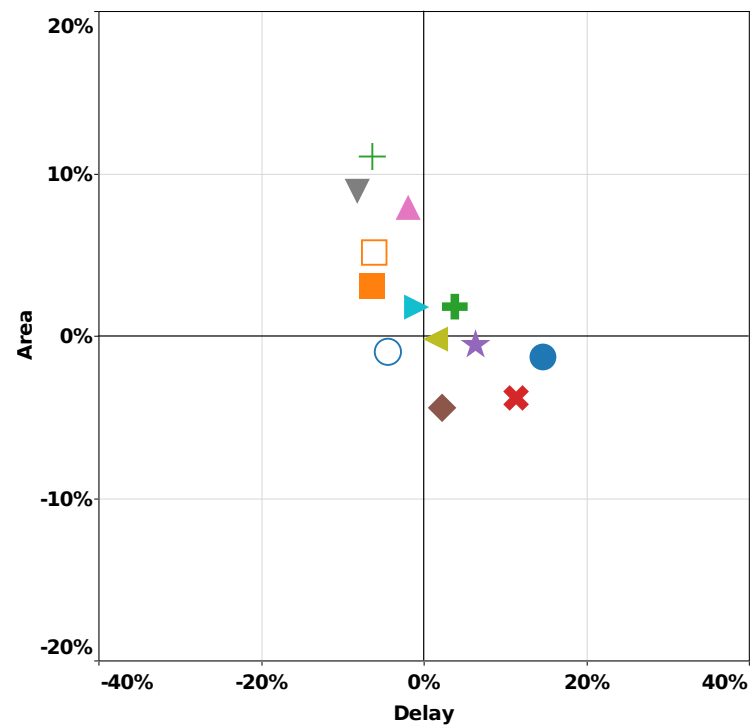
- K: Number of LUT inputs
- N: Number of BLEs
- I: Number of cluster inputs
- Complete input crossbar
- Delay optimization

Differences

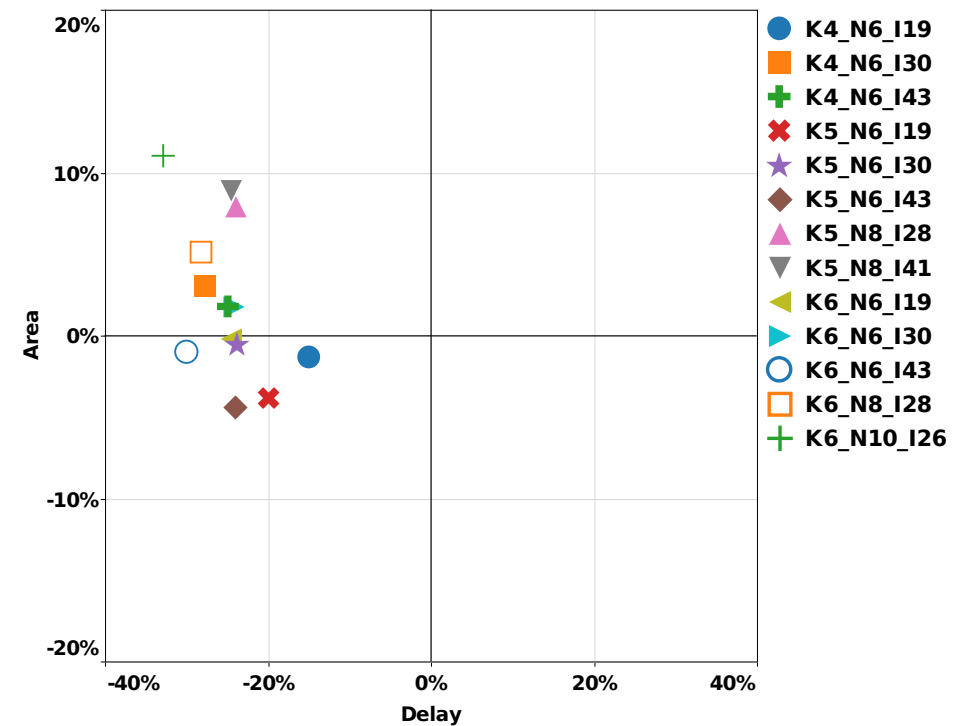
- No wire load models
- Estimated switch block capacitance

Results

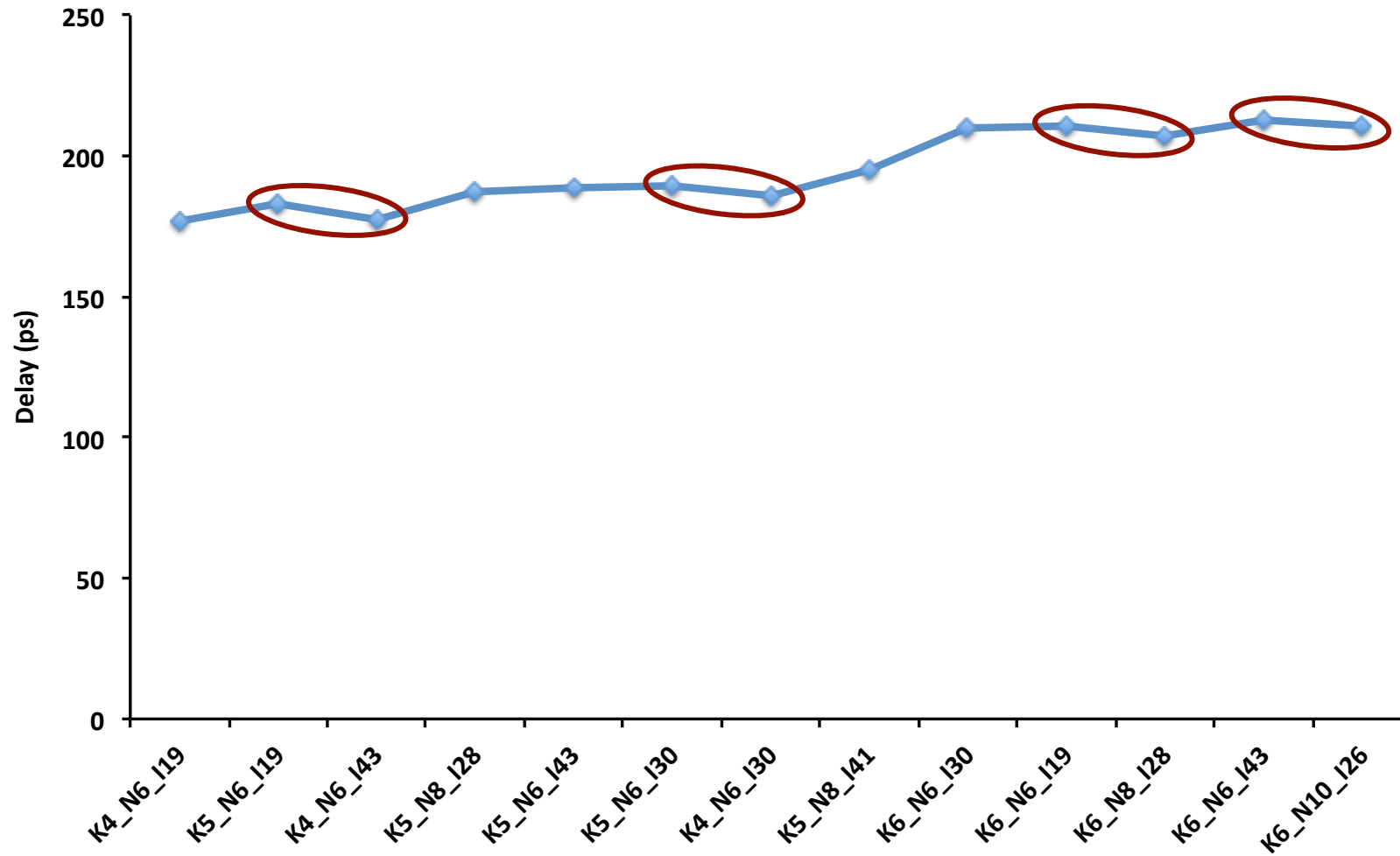
CLB's IO path



Feedback path

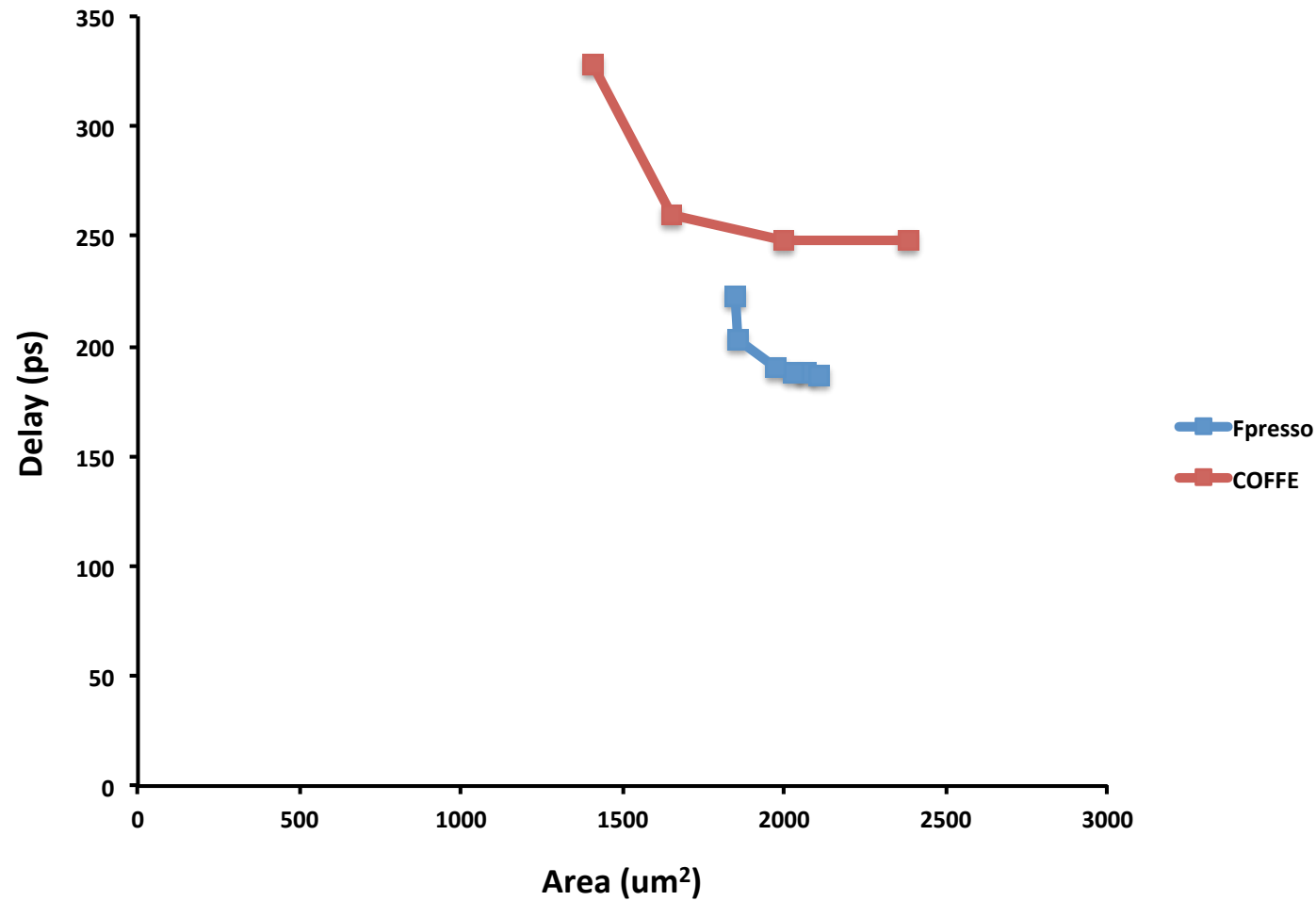


Fidelity of FPRESSO w.r.t. COFFE

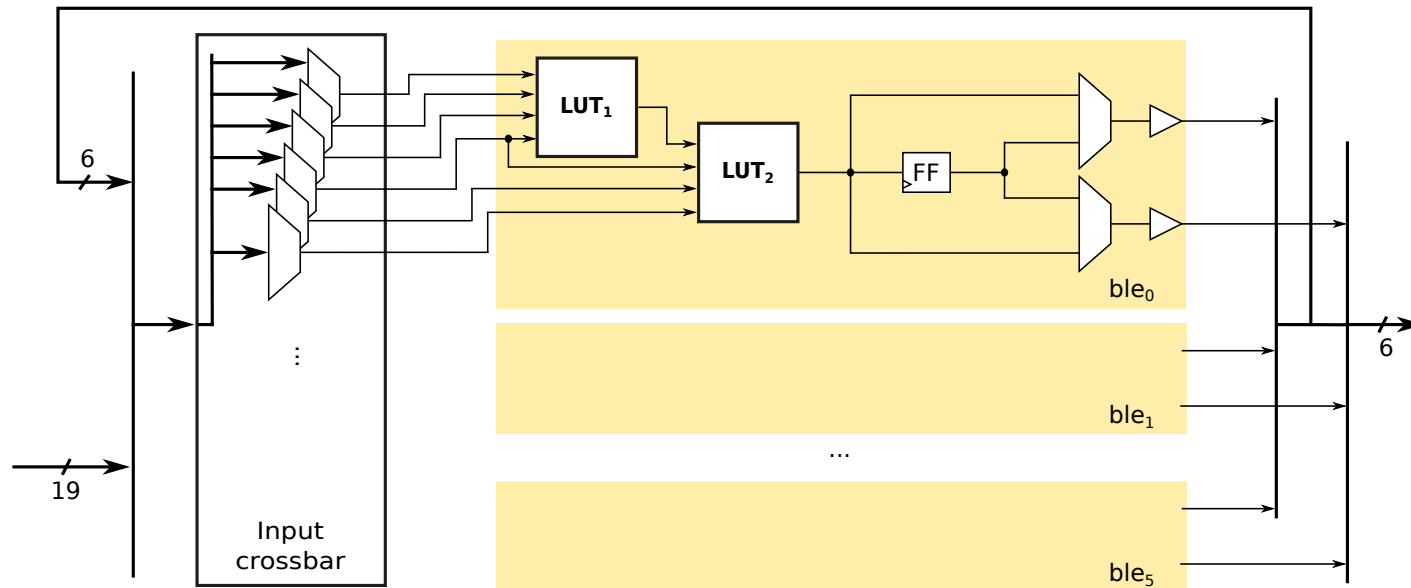


Area-Delay Pareto Front

Fixed architecture: $K = 5$, $N = 6$ and $I = 30$



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```

<pb_type name="clb" num_pb="1" num_in="19" num_out="6">
  <pb_type name="ble" num_pb="6" num_in="6" num_out="2">
    <pb_type name="lut1" num_pb="1" num_in="4" num_out="1"/>
    <pb_type name="lut2" num_pb="1" num_in="4" num_out="1"/>
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    <mux name="combseqfdb" input="ff.Q lut2.out" output="ble.out[0]"/>
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    <direct name="lutinA" input="ble.in[3:0]" output="lut1.in"/>
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    <direct name="lutinC" input="lut1.out" output="lut2.in[0]"/>
    <direct name="ffin" input="lut2.out" output="ff.D"/>
  </pb_type>
  <crossbar type="complete" name="inputxbar" input="clb.in ble.out[0]" output="ble.in"/>
  <direct name="bleout" input="ble.out[1]" output="clb.out"/>
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```

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