FPGA 2019 Sunday February 24

Time	Main Track		Deep Dive Track
8:45	**Welcome**	***Laguna Grande DEFG***	
9:00	**Tutorial (Chair: Stephen Neuendorffer)**	***Laguna Grande DEFG***	
9:00	The P4->NetFPGA Workflow for Line-Rate Packet Processing	Tutorial	
	Stephen Ibanez(2), Gordon Brebner(3), Nick McKeown(2), Noa Zilberman(1)		
	University of Cambridge(1), Stanford University(2), Xilinx Labs(3)		
10:00	**Break**	***Preconvene***	**Deep Dive**
10:15	Visual System Integrator	Invited Tutorial	***Laguna Grande C***
	Sandeep Dutta, Adnan Yunus, Artem Marisov, Matt Menezes, Somayeh Rahimipour: System View, Inc.		P4->NetFPGA
11:15	Build Your Own Domain-specific Solutions with RapidWright	Invited Tutorial	
	Chris Lavin, Alireza Kaviani: Xilinx, Inc.		
12:15	**Lunch**	***Atrium***	**Lunch**
13:45	**Machine Learning 1 (Chair: Jason Cong)**	***Laguna Grande DEFG***	RapidWright
13:45	Synetgy: Algorithm-hardware Co-design for ConvNet Accelerators on Embedded FPGAs		
	Yifan Yang(4, 3), Qijing Huang(3), Bichen Wu(3), Tianjun Zhang(3), Liang Ma(1), Giulio Gambardella(2),		
	Michaela Blott(2), Luciano Lavagno(1), Kees Vissers(2), John Wawrzynek(3), Kurt Keutzer(3)		
	Politecnico di Torino(1), Xilinx Research Labs(2), University of California, Berkeley(3), Tsinghua University(4)		
14:10	REQ-YOLO: A Resource-Aware, Efficient Quantization Framework for Object Detection on FPGAs		
	Caiwen Ding(3), Shuo Wang(2), Ning Liu(3), Kaidi Xu(3), Yanzhi Wang(3), Yun Liang(2, 1)		
	Peng Cheng Laboratory(1), Peking University(2), Northeastern University(3)		
14:35	Reconfigurable Convolutional Kernels for Neural Networks on FPGAs		
	Martin Hardieck, Martin Kumm, Konrad Moller, Peter Zipf		
	University of Kassel		
15:00	**Break**	***Preconvene***	**Break**
15:15	**Machine Learning 2 (Chair: Andrew Ling)**	***Laguna Grande DEFG***	RapidWright, continued
15:15	F5-HD: Fast Flexible FPGA-based Framework for Refreshing Hyperdimensional Computing		
	Sahand Salamat, Mohsen Imani, Behnam Khaleghi, Tajana Rosing		
	University of California, San Diego		
15:40	Efficient and Effective Sparse LSTM on FPGA with Bank-Balanced Sparsity		
	Shijie Cao(3), Chen Zhang(4), Zhuliang Yao(1), Wencong Xiao(2), Lanshun Nie(3), Dechen Zhan(3), Yunxin Liu(4), Ming Wu(4), Lintao Zhang(4)		
	Tsinghua University(1), Beihang University(2), Harbin Institute of Technology(3), Microsoft Research(4)		
16:05	Cloud-DNN: An Open Framework for Mapping DNN Models to Cloud FPGAs		
	Yao Chen(1), Jiong He(1), Xiaofan Zhang(2), Cong Hao(2), Deming Chen(2, 1)		
	Advanced Digital Sciences Center(1), University of Illinois at Urbana-Champaign(2)		
16:30	**Adjourn**		**Adjourn**
16:30	**FCCM PC meeting**	***Big Sur***	
19:00	**Reception**	***Laguna Grande ABC***	

FPGA 2019 Monday February 25

Time	Main Track	
8:45	**Keynote (Chair: John Lockwood)**	***Laguna Grande DEFG***
8:45	Versal: The Xilinx Adaptive Compute Acceleration Platforms (ACAP)	Keynote
	Kees Vissers: Xilinx, Inc.	
9:15	**Computing Architectures (Chair: John Lockwood)**	***Laguna Grande DEFG***
9:15	Xilinx Adaptive Compute Acceleration Platform: Versal Architecture	
	Brian Gaide, Dinesh Gaitonde, Chirag Ravishankar, Trevor Bauer: Xilinx, Inc.	
9:40	Math Doesn't Have to be Hard: Logic Block Architectures to Enhance Low Precision Multiply-Accumulate on FPGAs	
	Andrew Boutros(1, 2), Mohamed Eldafrawy(1), Sadegh Yazdanshenas(1), Vaughn Betz(1, 2)	
	University of Toronto(1), Vector Institute(2)	
10:05	LANMC: LSTM-Assisted Non-Rigid Motion Correction on FPGA for Calcium Image Stabilization	Short Paper
	Zhe Chen, Hugh Blair, Jason Cong: University of California, Los Angeles	
10:10	On-chip FPGA Debug Instrumentation for Machine Learning Applications	Short Paper
	Daniel Holanda Noronha(3), Ruizhe Zhao(2), Jeff Goeders(1), Wayne Luk(2), Steven Wilton(3)	
	Brigham Young University(1), Imperial College London(2), University of British Columbia(3)	
10:15	**Break and Poster Session 1 (Chair: George Constantinides)**	***Preconvene/Seaside***
11:25	**CAD (Chair: Sinan Kaptonoglu)**	***Laguna Grande DEFG***
11:25	Multi-Commodity Flow-Based Spreading in a Commercial Analytic Placer	Best Paper Candidate
	Nima Karimpour Darav(2), Andrew Kennings(1), Kristofer Vorwerk(2), Arun Kundu(2)	
	University of Waterloo(1), Microsemi Corporation(2)	
11:50	Simultaneous Placement and Clock Tree Construction for Modern FPGAs	
	Wuxi Li(1), Mehrdad Dehkordi(2), Stephen Yang(2), David Pan(1)	
	University of Texas at Austin(1), Xilinx, Inc.(2)	
12:15	EASY: Efficient Arbiter SYnthesis from Multi-threaded Code	
	Jianyi Cheng(2), Shane Fleming(2), Yu Ting Chen(1), Jason Anderson(1), George Constantinides(2)	
	University of Toronto(1), Imperial College London(2)	
12:40	**Lunch**	***Atrium***
14:10	**Synthesis (Chair: Martin Langhammer)**	***Laguna Grande DEFG***
14:10	Substream-Centric Maximum Matchings on FPGA	Best Paper Candidate
	Maciej Besta, Marc Fischer, Tal Ben-Nun, Johannes De Fine Licht, Torsten Hoefler: ETH Zurich	
14:35	Speculative Dataflow Circuits	
	Lana Josipovic, Andrea Guerrieri, Paolo Ienne: EPFL	
15:00	Constructing Concurrent Data Structures on FPGA with Channels	Short Paper
	Hui Yan, Zhaoshi Li, Leibo Liu, Shouyi Yin, Shaojun Wei: Tsinghua University	
15:05	Rapid Cycle-Accurate Simulator for High-Level Synthesis	Short Paper
	Yuze Chi, Young-kyu Choi, Jason Cong, Jie Wang: UCLA	
15:10	**Break and Poster Session 2 (Chair: Phillip Leong)**	***Preconvene/Seaside***
16:20	**Tutorial (Chair: Phillip Leong)**	***Laguna Grande DEFG***
16:20	Compute-Efficient Neural-Network Acceleration	Tutorial
	Ephrem Wu, Xiaoqian Zhang, David Berman, Inkeun Cho, John Thendean: Xilinx, Inc.	
17:20	**Adjourn**	
18:30	**Banquet and Panel**	***Laguna Grande ABC***

FPGA 2019 Tuesday February 26

Time	Main Track	
8:45	**Tutorial (Chair: Alireza Kaviani)**	***Laguna Grande DEFG***
8:45	Fractal Synthesis	Invited Tutorial
	Martin Langhammer, Gregg Baeckler, Sergey Gribok: Intel PSG	
9:45	**Networks and NOCs (Chair: Grace Zgheib)**	***Laguna Grande DEFG***
9:45	Network-on-Chip Programmable Platform in Versal™ ACAP Architecture	
	Ian Swarbrick, Dinesh Gaitonde, Sagheer Ahmad, Brian Gaide, Ygal Arbel: Xilinx, Inc.	
10:10	HopliteBuf: FPGA NoCs with Provably Stall-Free FIFOs	Best Paper Candidate
	Tushar Garg, Saud Wasly, Rodolfo Pellizzoni, Nachiket Kapre: University of Waterloo	
10:35	The Network Management Unit (NMU): Securing Network Access for Direct-Connected FPGAs	
	Daniel Rozhko, Paul Chow: University of Toronto	
11:00	**Break**	***Preconvene***
11:15	**Heterogenous Platforms (Chair: Vinod Kathail)**	***Laguna Grande DEFG***
11:15	HeteroCL: A Multi-Paradigm Programming Infrastructure for Software-Defined Reconfigurable Computing	Best Paper Candidate
	Yi-Hsiang Lai(1), Yuze Chi(2), Yuwei Hu(1), Jie Wang(2), Cody Hao Yu(2, 3), Yuan Zhou(1), Jason Cong(2), Zhiru Zhang(1)	
	Cornell University(1), University of California, Los Angeles(2), Falcon Computing Solutions, Inc.(3)	
11:40	AFFIX: Automatic Acceleration Framework for FPGA Implementation of OpenVX Vision Algorithm	
	Sajjad Taheri(2), Payman Behnam(1), Eli Bozorgzadeh(2), Alexander Veidenbaum(2), Alexandru Nicolau(2)	
	University of Utah(1), University of California, Irvine(2)	
12:05	A Modular Heterogeneous Stack for Deploying FPGAs and CPUs in the Data Center	
	Nariman Eskandari, Naif Tarafdar, Daniel Ly-Ma, Paul Chow: University of Toronto	
12:30	**Lunch**	***Atrium***
14:00	**Devices and Security (Chair: Jeffrey Goeders)**	***Laguna Grande DEFG***
14:00	Impact of Soft Errors on Large-Scale FPGA Cloud Computing	
	Andrew Keller, Michael Wirthlin: Brigham Young University	
14:25	Breaking the Trust Dependence on Third Party Processes for Reconfigurable Secure Hardware	
	Aimee Coughlin, Greg Cusack, Jack Wampler, Eric Keller, Eric Wustrow: University of Colorado, Boulder	
14:50	Characterization of Long Wire Data Leakage in Deep Submicron FPGAs	Short Paper
	George Provelengios(1), Chethan Ramesh(1), Shivukumar Patil(1), Ken Eguro(2), Russell Tessier(1), Daniel Holcomb(1)	
	University of Massachusetts Amherst(1), Microsoft Research(2)	
14:55	Temporal Thermal Covert Channels on Cloud FPGAs	Short Paper
	Shanquan Tian, Jakub Szefer: Yale University	
15:00	**Break and Poster Session 3 (Chair: Kees Vissers)**	***Preconvene/Seaside***
16:10	**Memory (Chair: Herman Schmit)**	***Laguna Grande DEFG***
16:10	Stop Crying Over Your Cache Miss Rate: Handling Efficiently Thousands of Outstanding Misses in FPGAs	
	Mikhail Asiatici, Paolo Ienne: EPFL	
16:35	Improving Performance of Graph Processing on FPGA-DRAM Platform by Two-level Vertex Caching	
	Zhiyuan Shao, Ruoshi Li, Diqing Hu, Xiaofei Liao, Hai Jin: Huazhong University of Science and Technology	
17:00	FASED: FPGA-Accelerated Simulation and Evaluation of DRAM	
	David Biancolin(2), Sagar Karandikar(1), Donggyu Kim(2, 1), Jack Koenig(2), Andrew Waterman(2), Jonathan Bachrach(2), Krste Asanovic(2)	
	SiFive Inc.(1), University of California, Berkeley(2)	
17:25	**Best Paper Award**	
17:35	**Adjourn**	