



# Packet Matching on FPGAs Using HMC Memory: Towards One Million Rules

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# Motivation

- Packet processing is used to decide what to do with incoming packets to a network device
  - Check packets against a list of rules (rulesets)

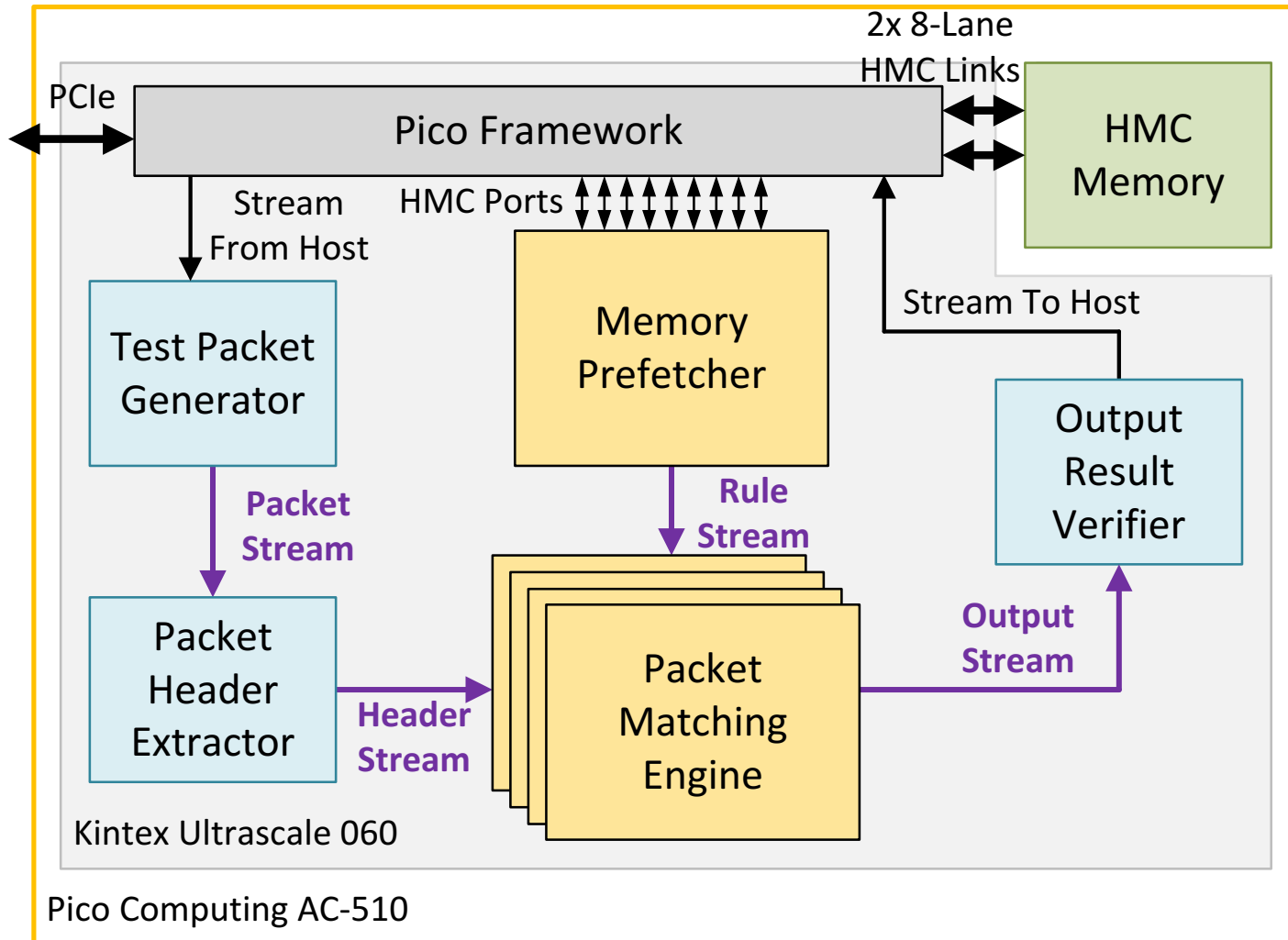
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- **Certain applications need very large rulesets**
  - On-chip FPGA implementations support a limited number of rules (<10K)
  - Traditional off-chip memory is too slow

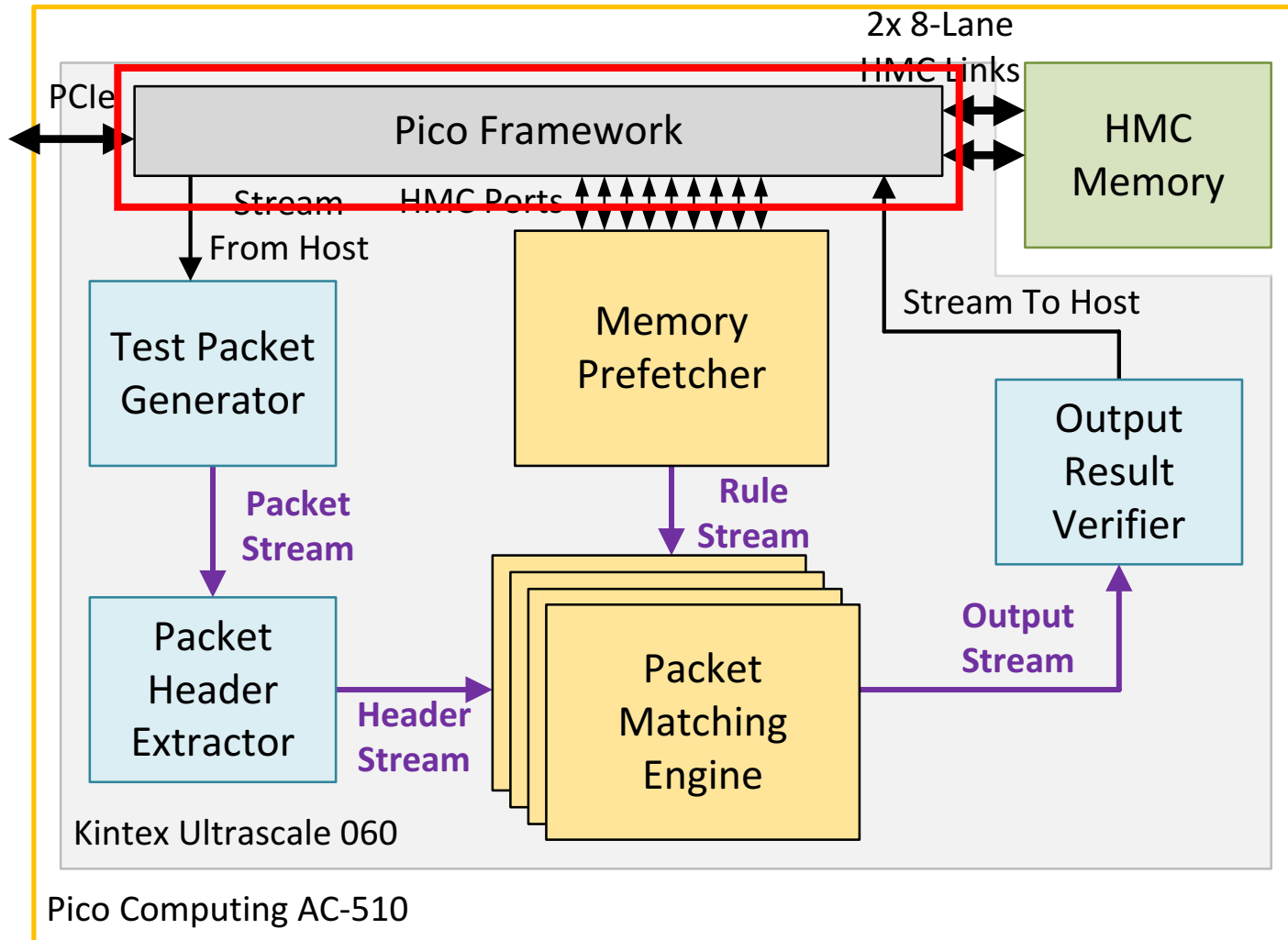
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- Emerging high performance memories like Hybrid Memory Cube (HMC) could be a solution
  - 10G line rate at 1 million rules

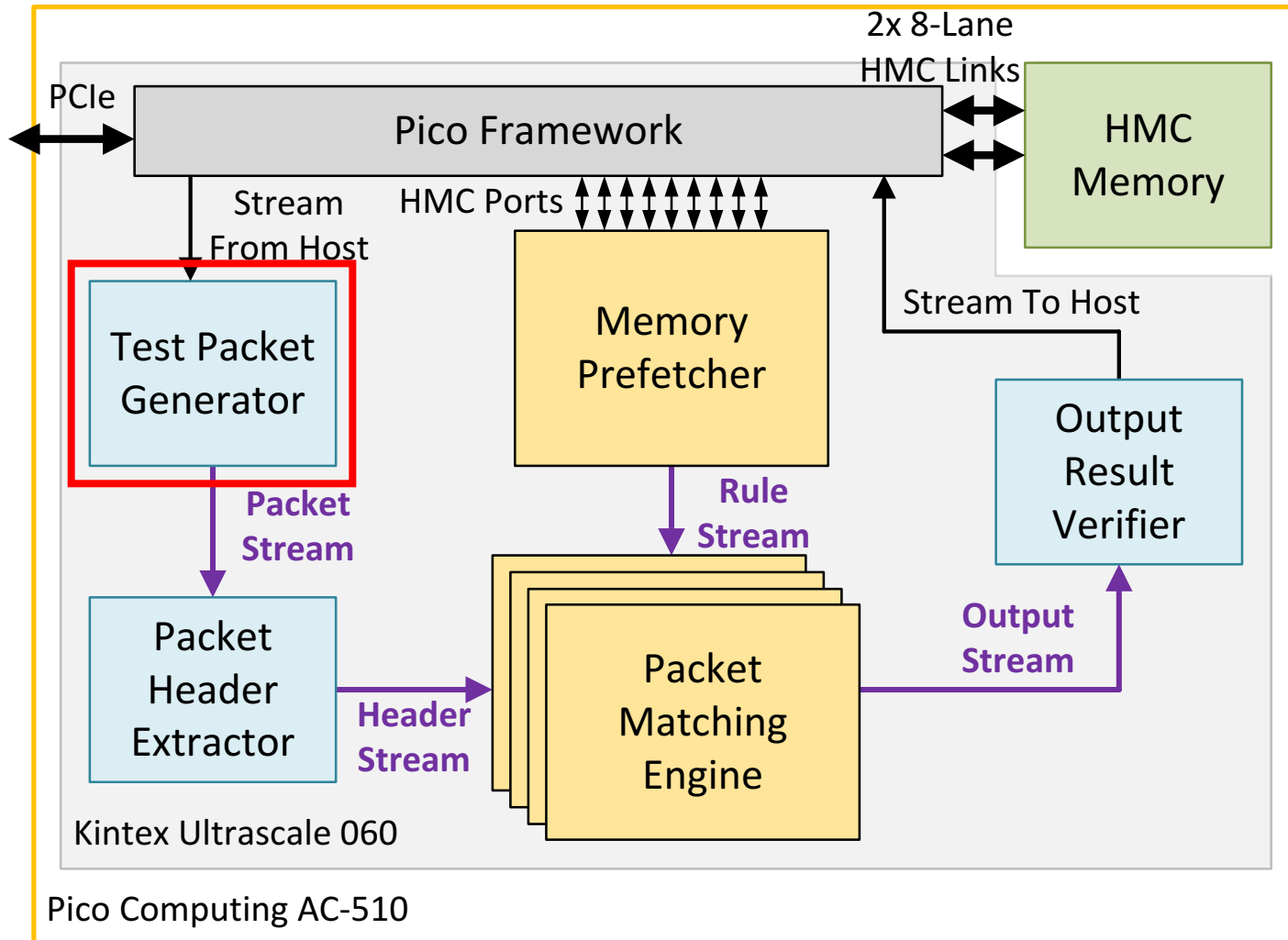
# System Architecture



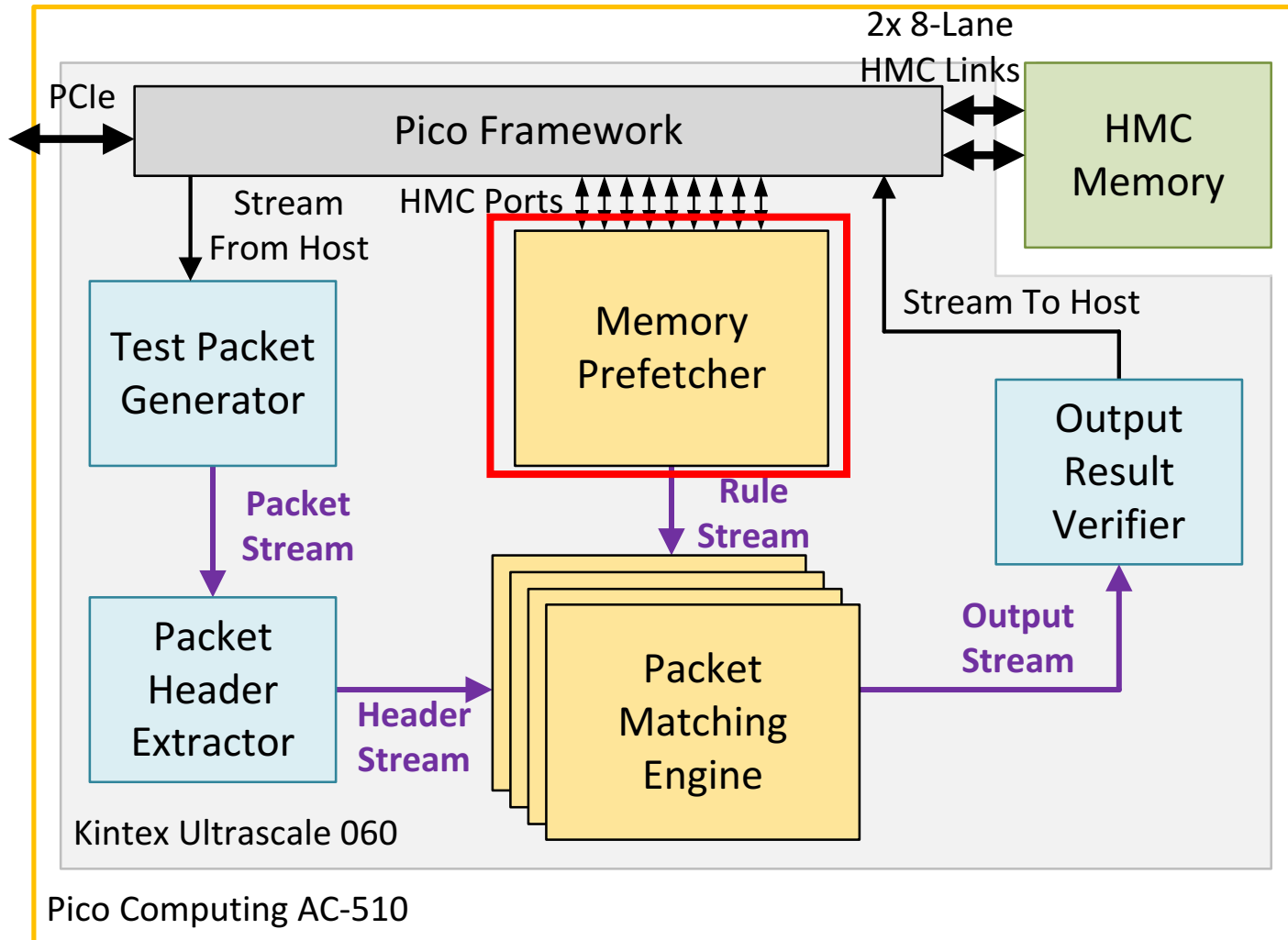
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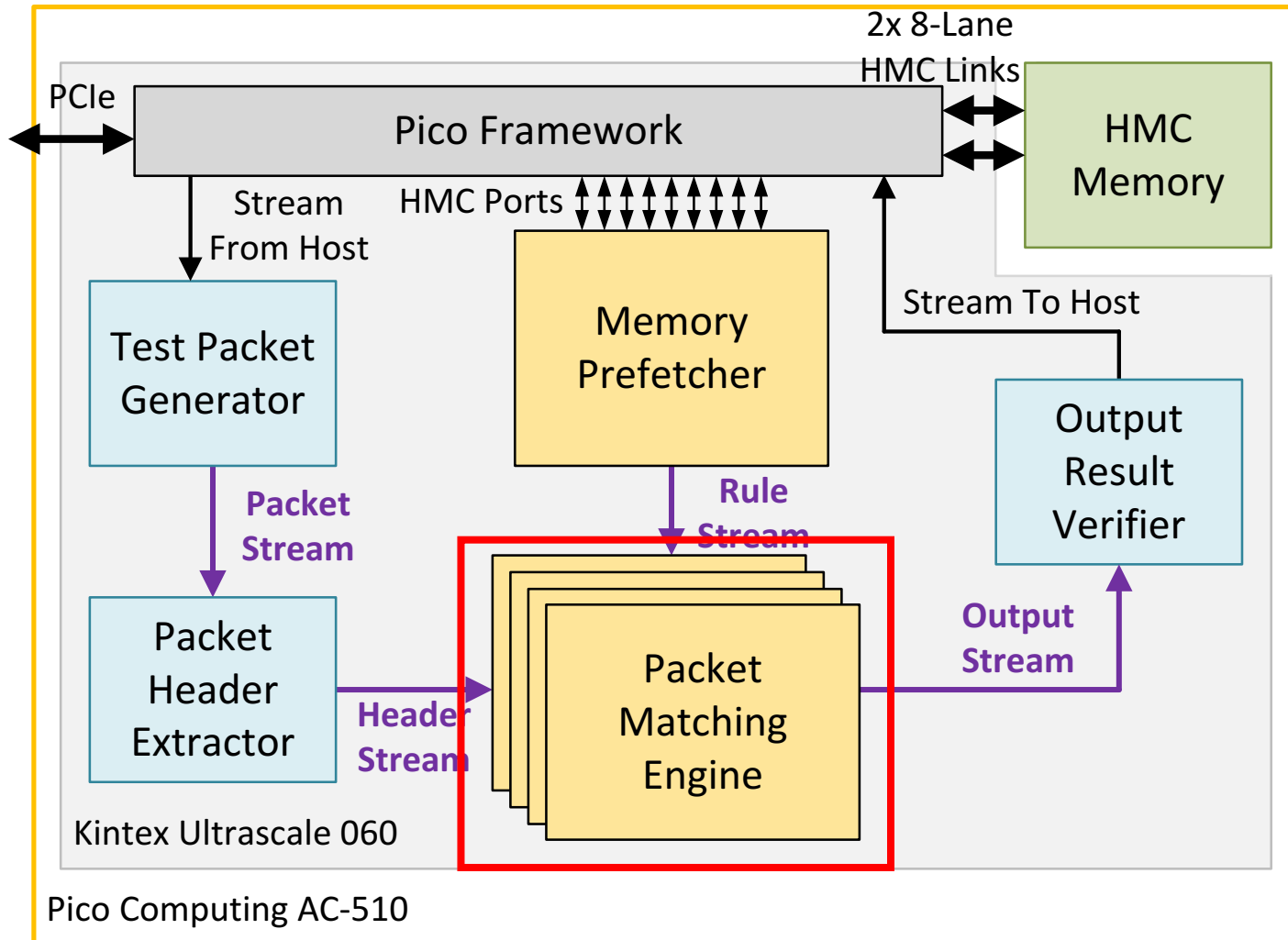


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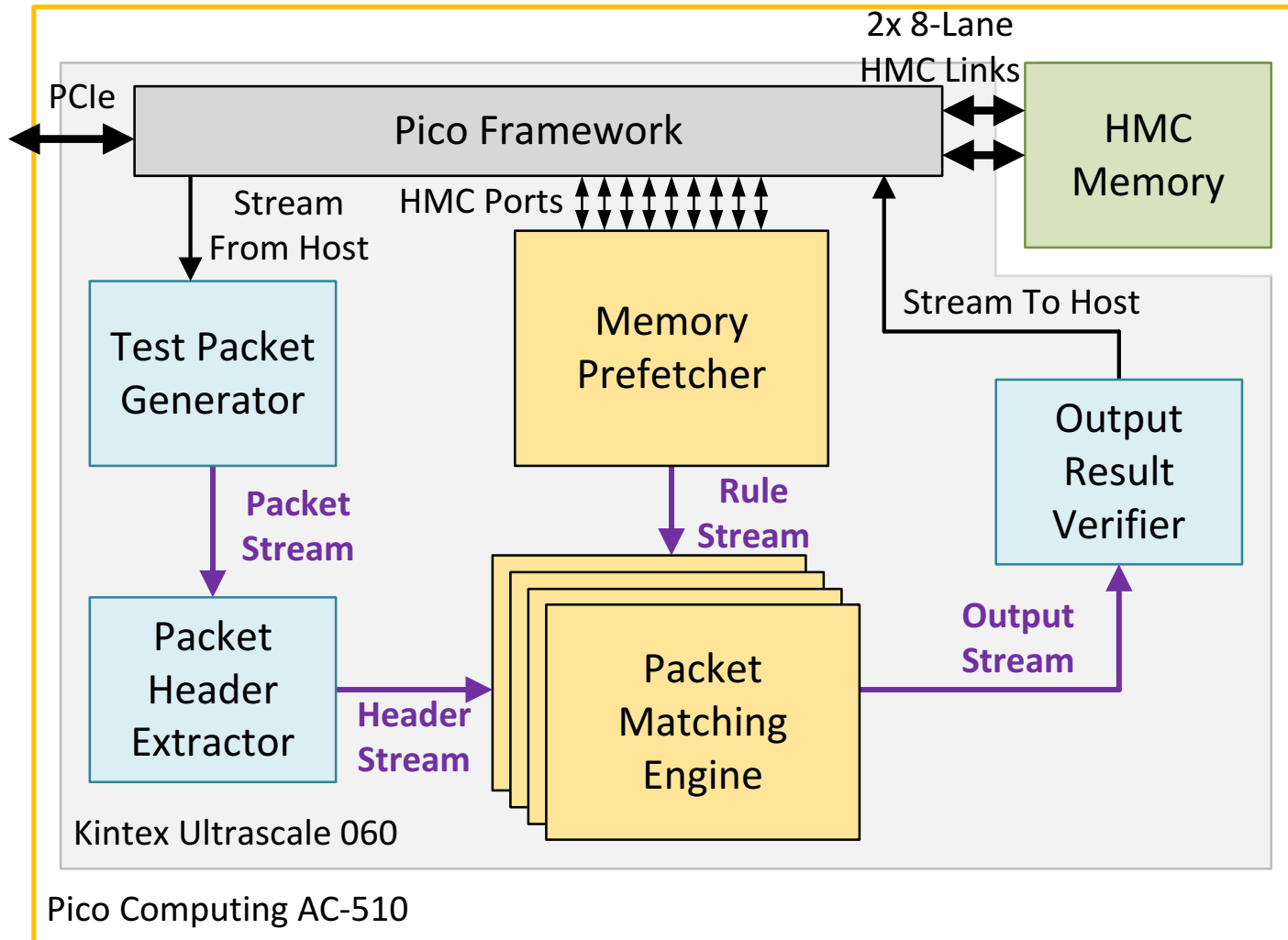




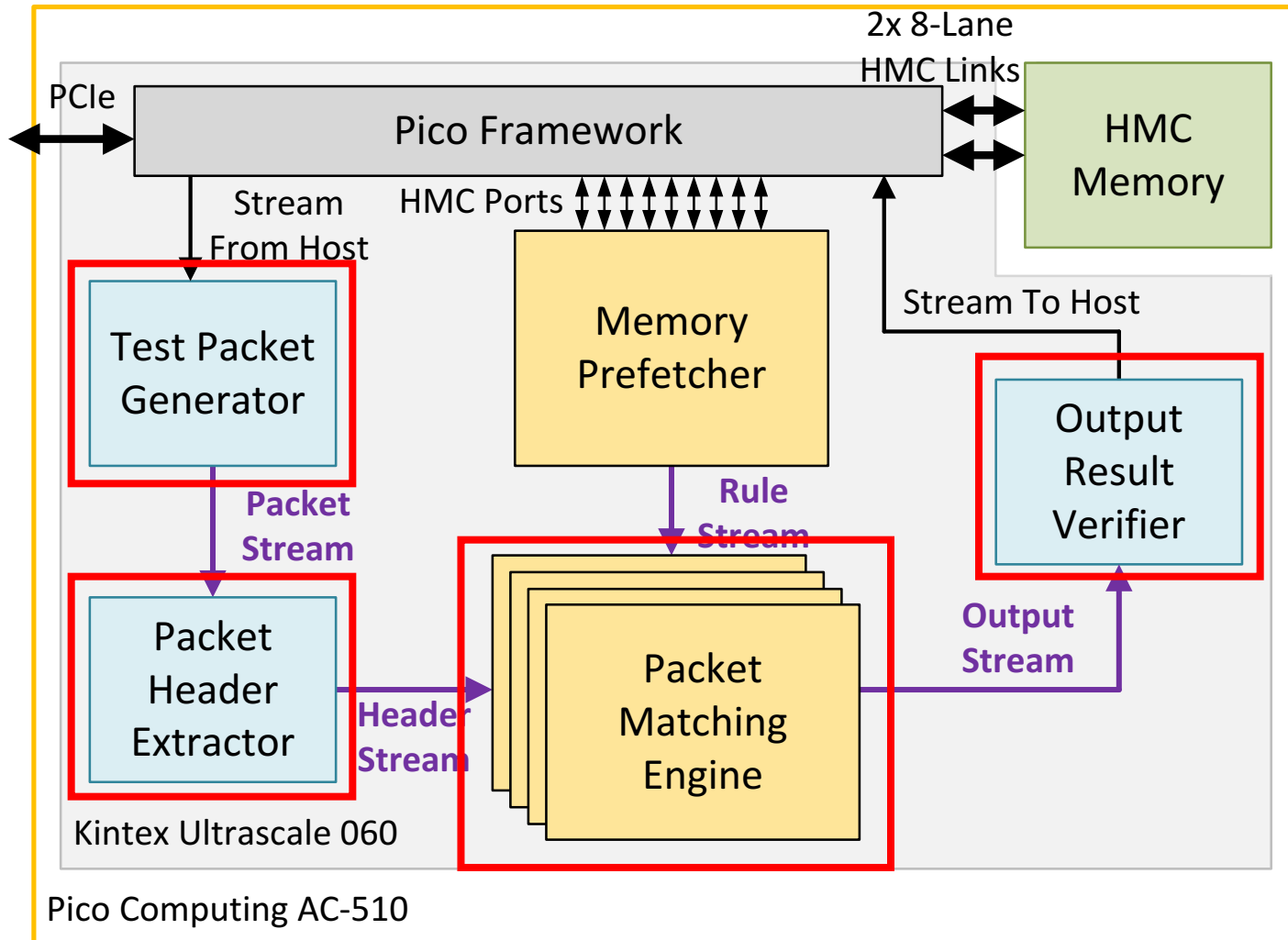
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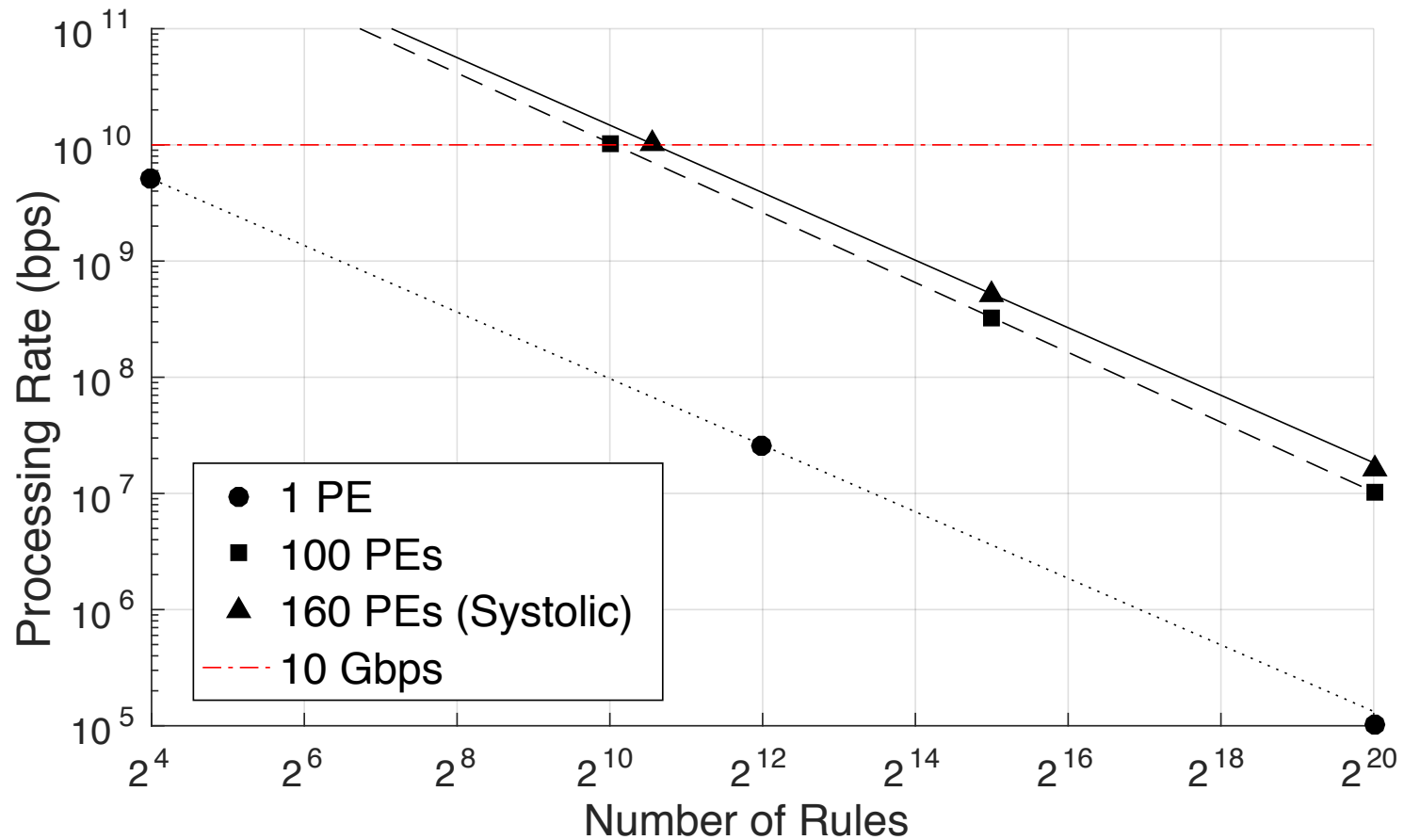
# Experience with HLS



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# Results - Throughput





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