0.5-V Highly Power-Efficient Programmable Logic using Nonvolatile Configuration Switch in BEOL

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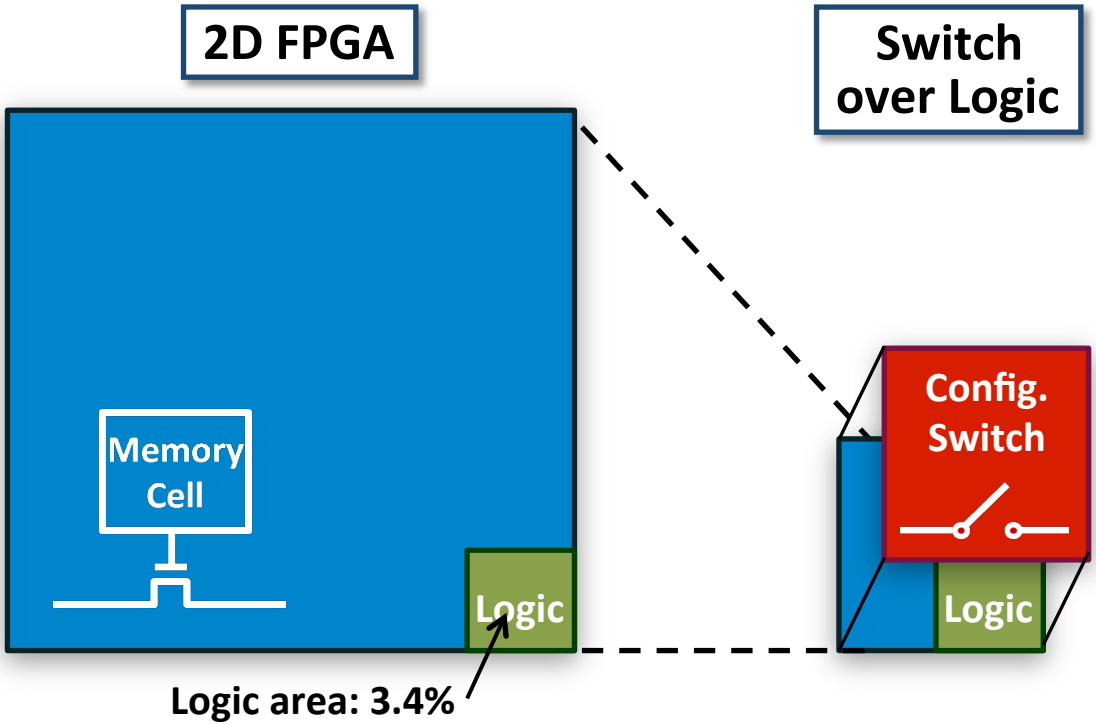
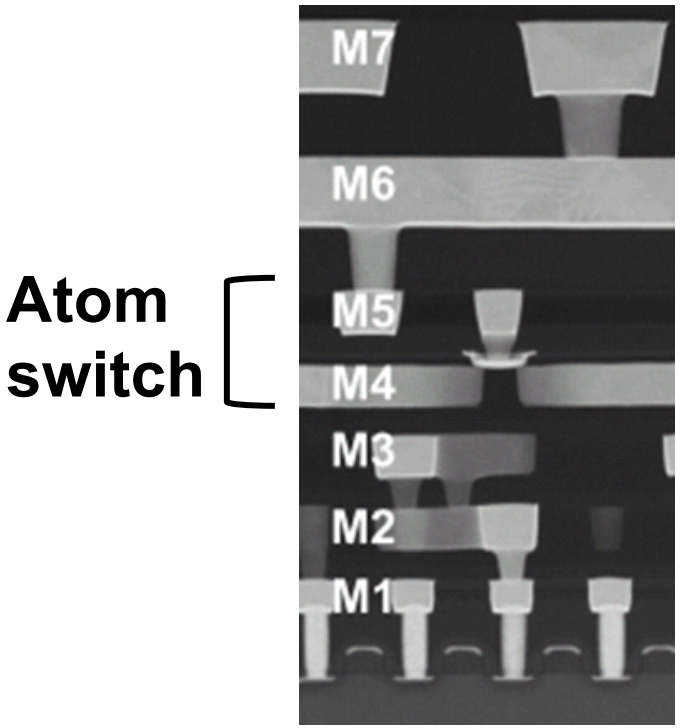
Concept of "Switch Over Logic"

- Nonvolatile switch is stacked on logic plane
  - Reduced cell area (Stacked switch plane)
  - Low Power (Nonvolatility / Shorter wiring length)
  - Complementary Atom SW reduces programming voltage

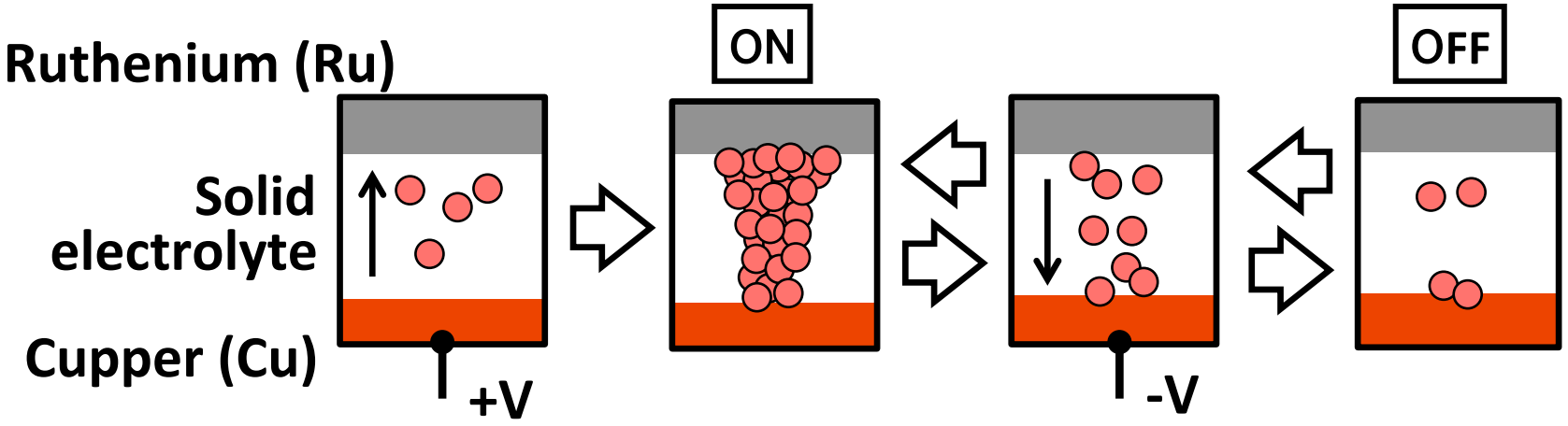




(*1) I.Kuon & J.Rose, IEEE CAD, 2007

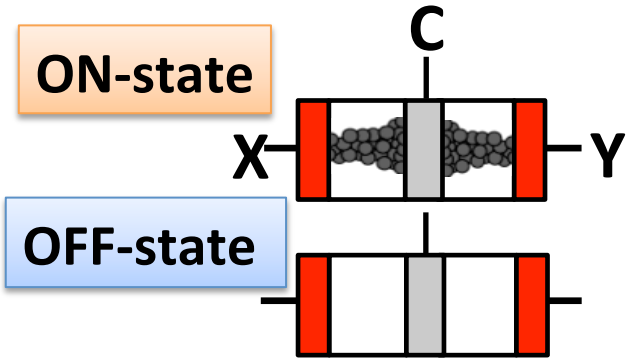
Operation principle

- Atom switch : Nanometer-scale Cu bridge forms between two electrodes via electrochemical reaction.

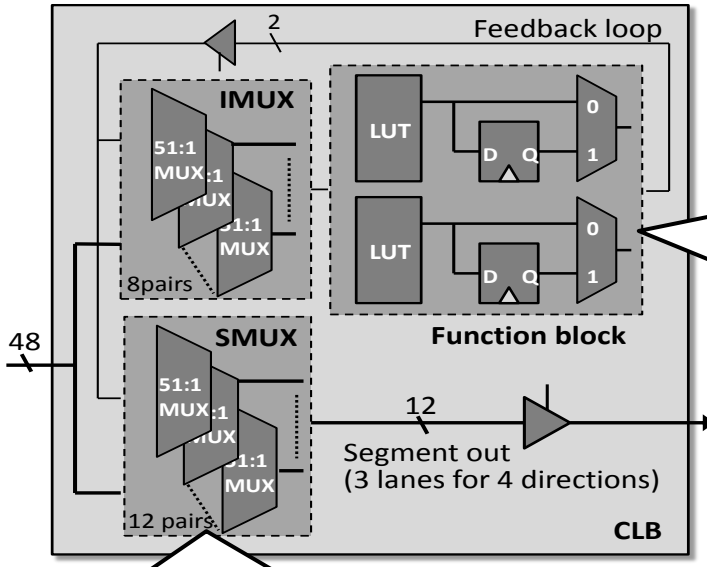


- Features
  - Nonvolatile
  - Small input capacitance (1/10 of CMOS)
  - Rewritable (>10^3)
  - BEOL integration (small area)

Complementary Atom Switch (CAS)



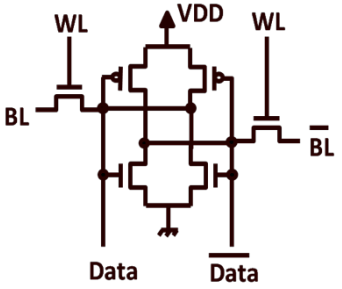
CAS-based Configurable Logic Block

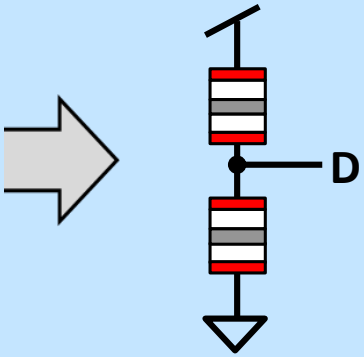


CAS-based memories

- Nonvolatile

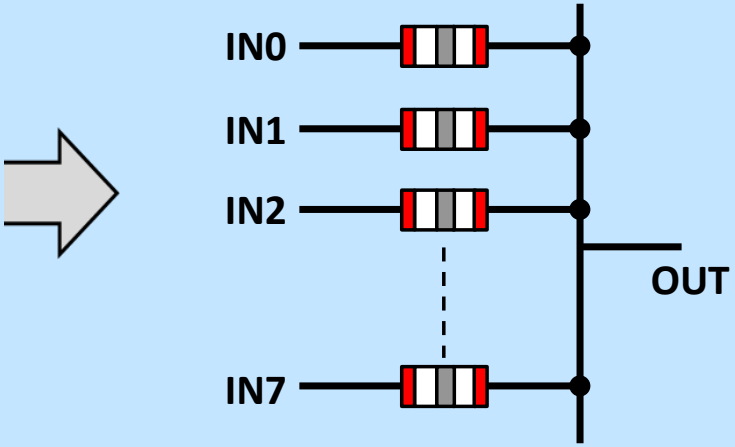
Conventional SRAM





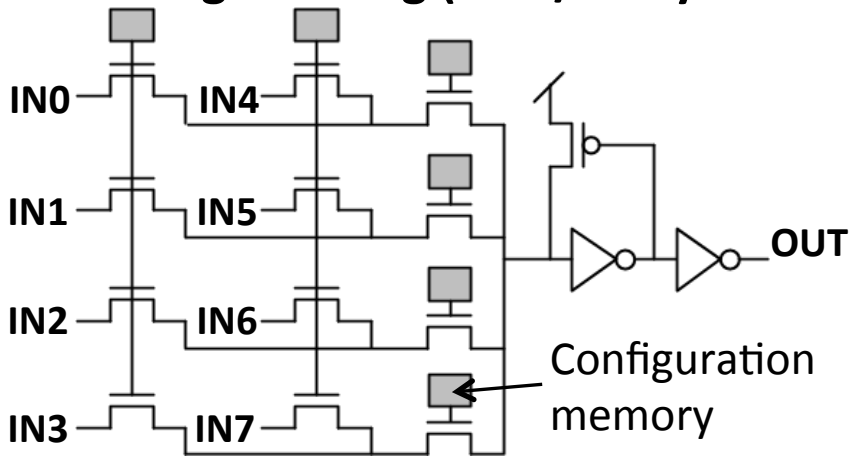
CAS-based MUX

- Single-stage routing
- Small Cin (0.14fF/CAS)



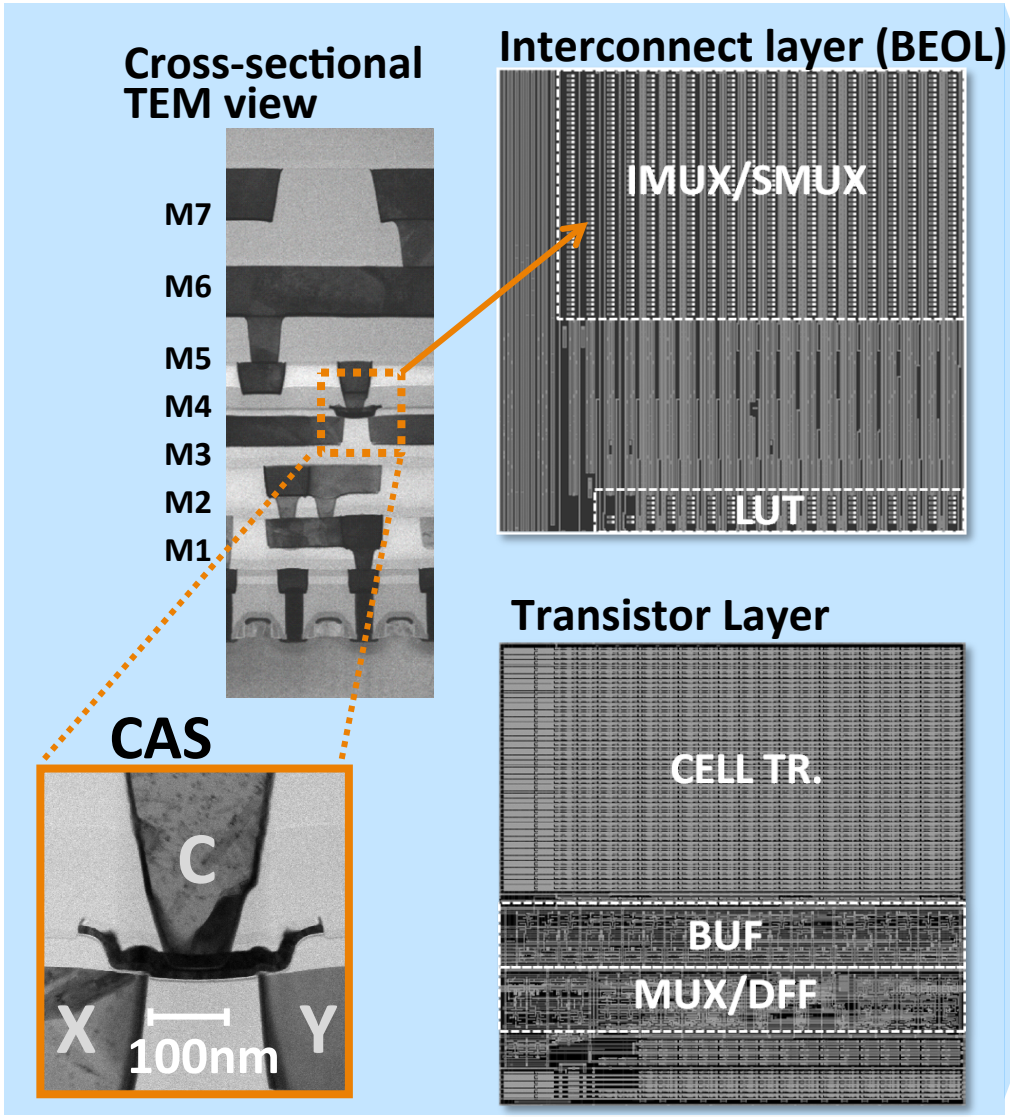
Conventional MUX

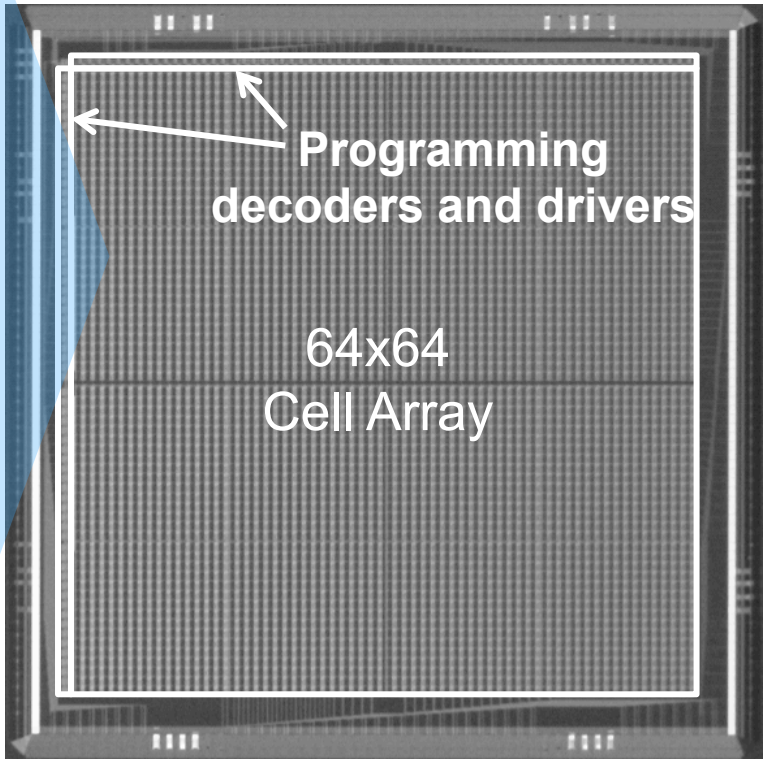
- Multi-stage routing (area/delay tradeoff)



Physical implementation

- CASs are embedded in M4-M5 with 65nm-node CMOS process.
  - 2 additional masks for CAS
  - M1-5 local metal
  - M6-7 semi-global metal

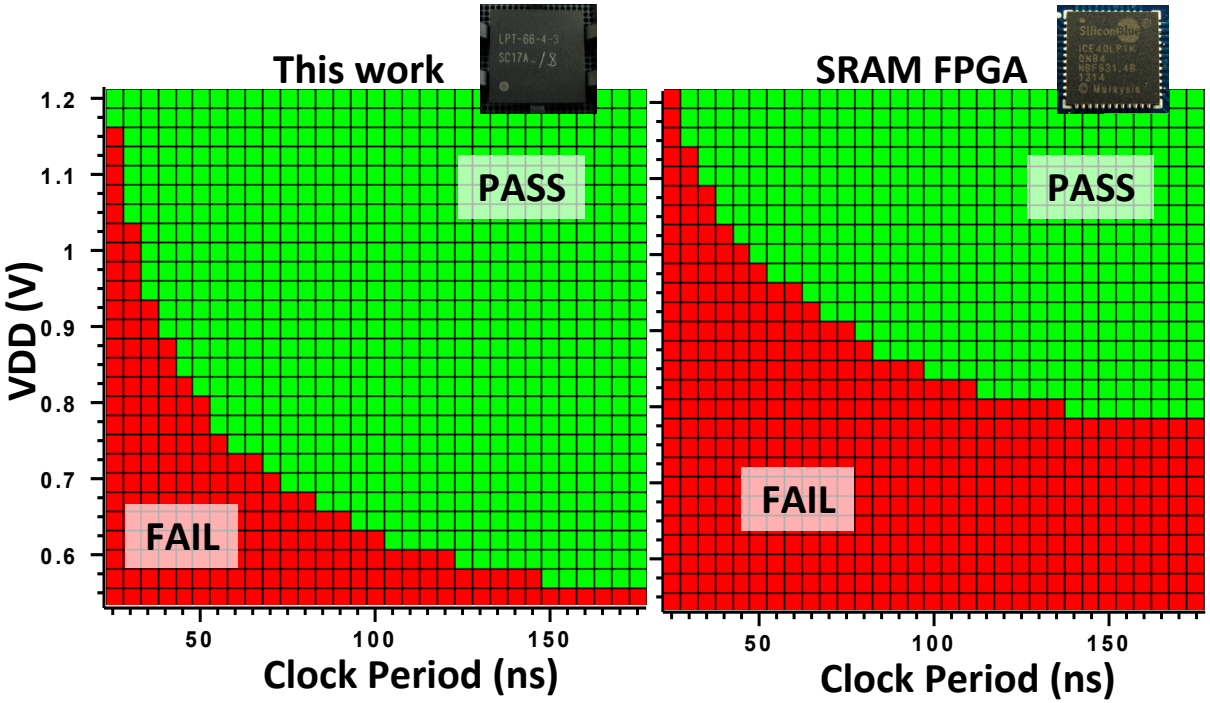




4.6M-bit CAS integrated

Low power/high performance of AtomSW-FPGA

- Comparison with commercial low-power FPGA
  - 64x64 AtomSW-FPGA vs SRAM-based FPGA
  - 16b-ALU/Signal-generator are mapped using 332 LUTs.
  - Dynamic power : -30% at minimum operating voltage
  - Critical path delay : -60% for VDD=0.8V



	AtomSW FPGA	SRAM FPGA*
Routing SW	AtomSW	SRAM, Pass Tr.
Process node	65nm	40nm
# of LUTs	8192	1280
Max. speed @0.8V	18.2MHz	7.1MHz
VDDmin @15MHz	0.73V	0.94V
Dynamic power @ VDDmin	28.0 µW/ MHz	39.5 µW/ MHz
Active power @ VDDmin	550µW	630µW

**http://www.latticesemi.com/Products/FPGAandCPLD/iCE40.aspx*

Acknowledgements

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