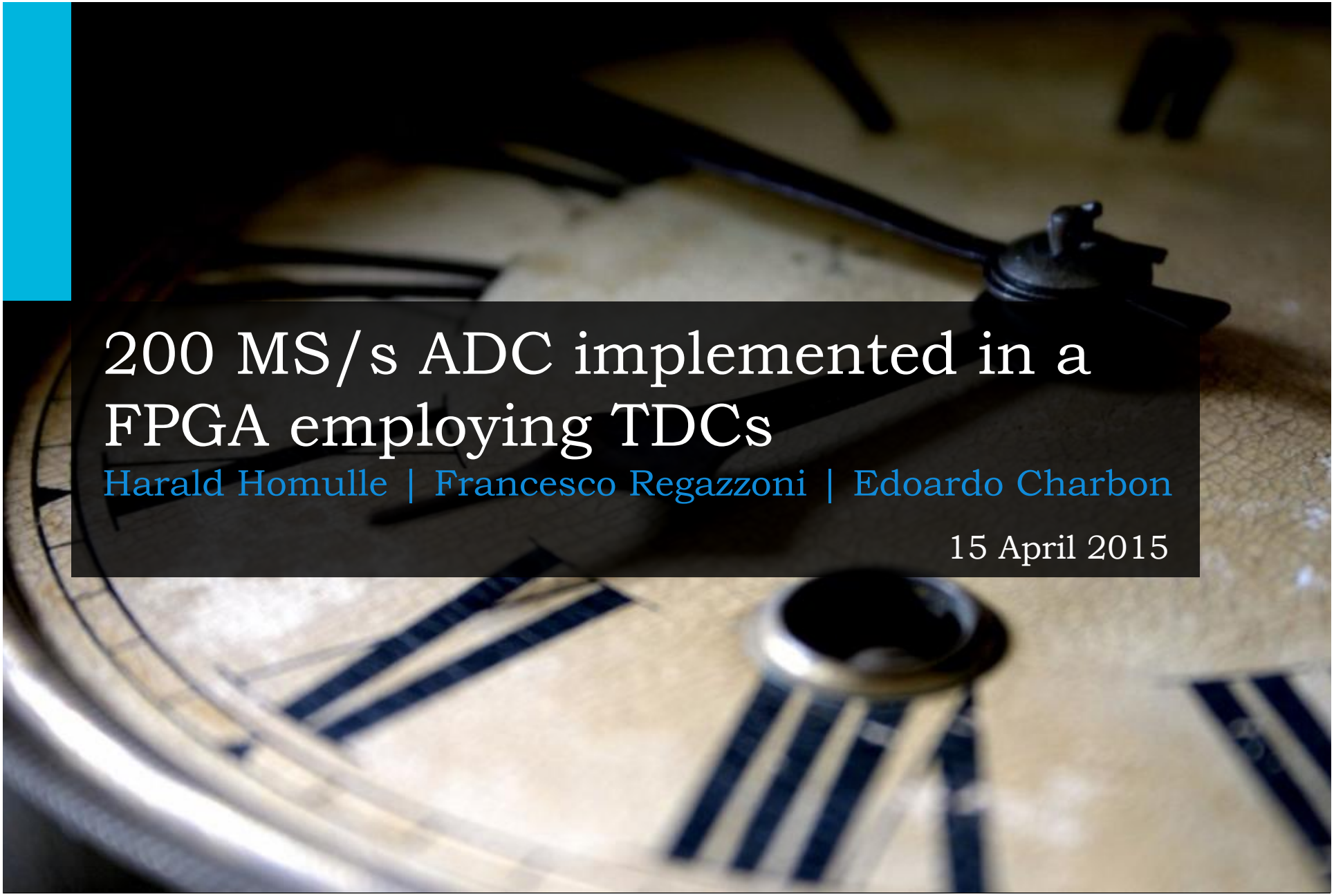


# 200 MS/s ADC implemented in a FPGA employing TDCs

Harald Homulle | Francesco Regazzoni | Edoardo Charbon

15 April 2015

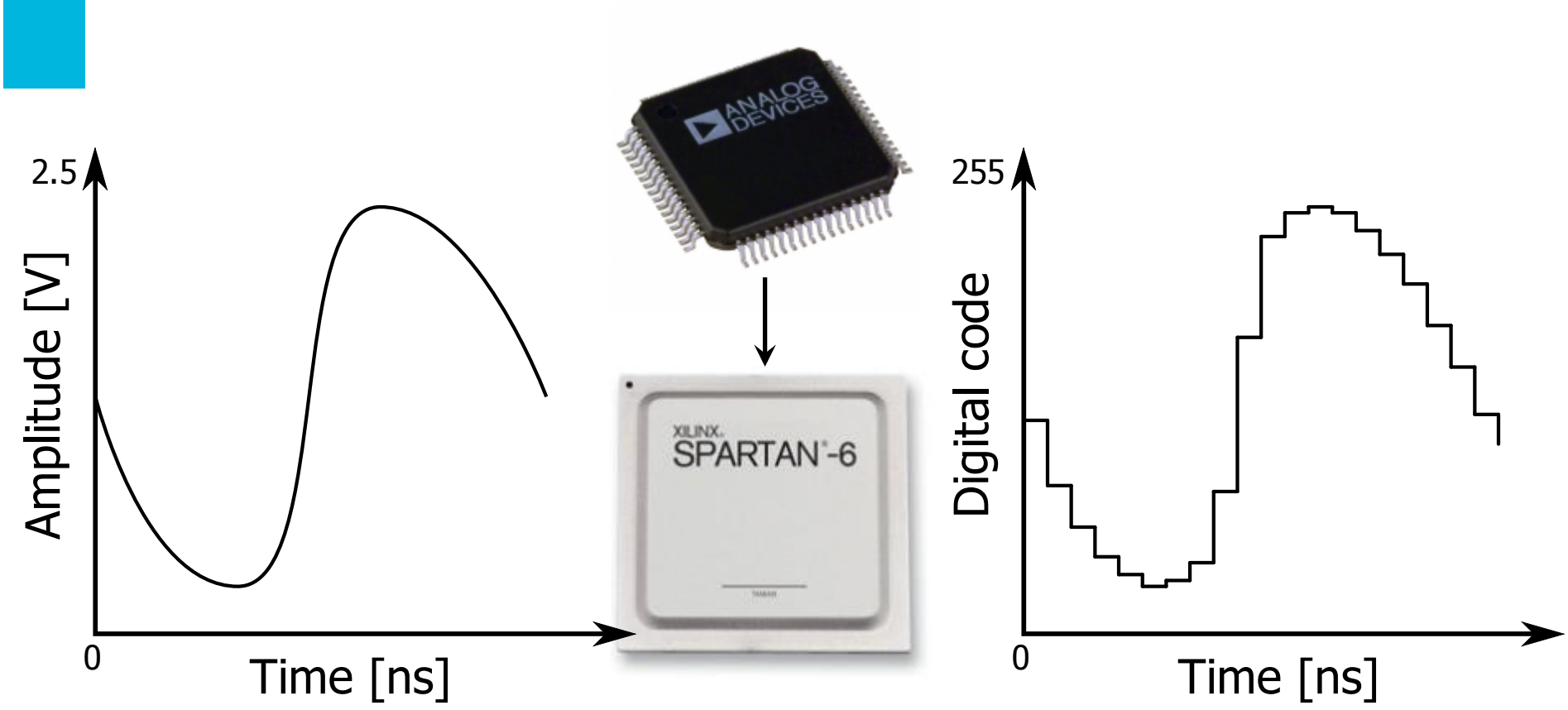
# Contents

## Developing FPGA ADCs

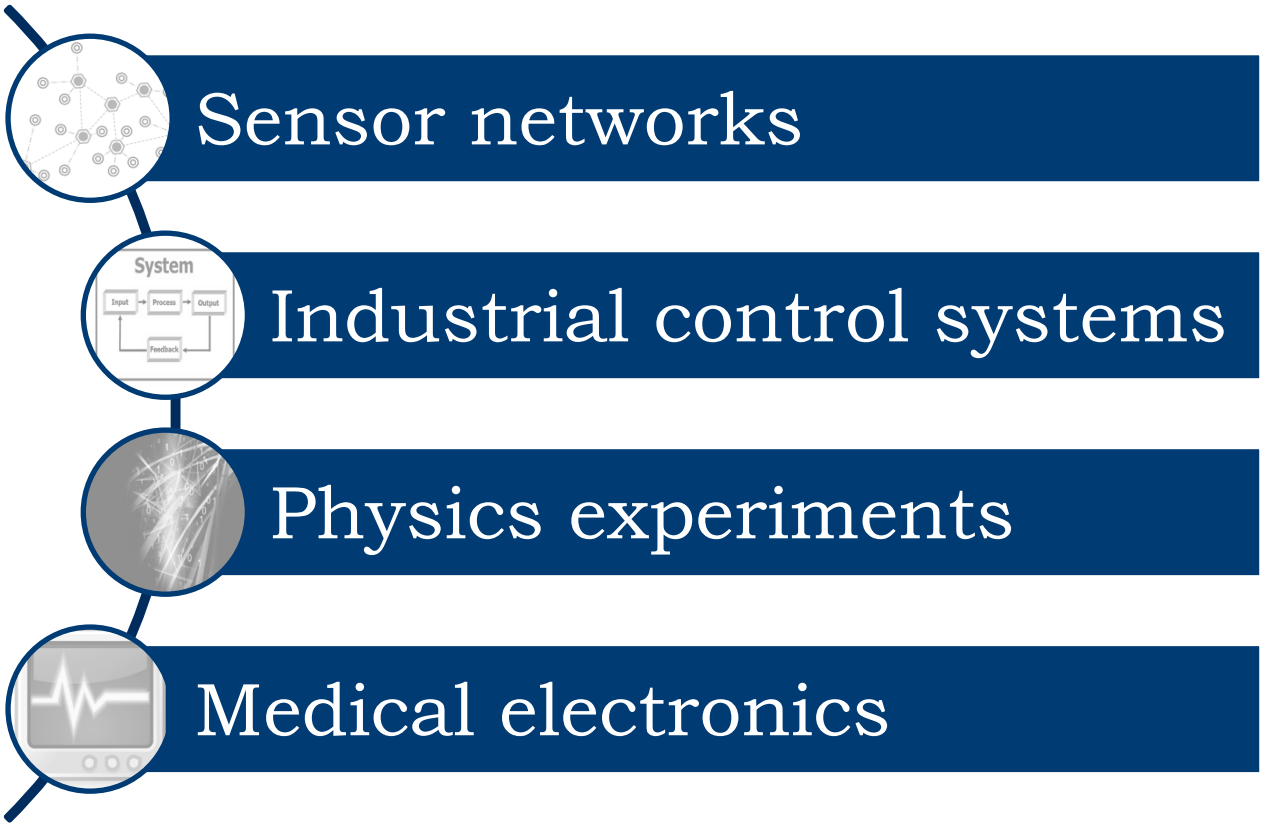
- Introduction
- System Architecture
- Results
- Conclusion

# 1. INTRODUCTION

# FPGA ADCs?

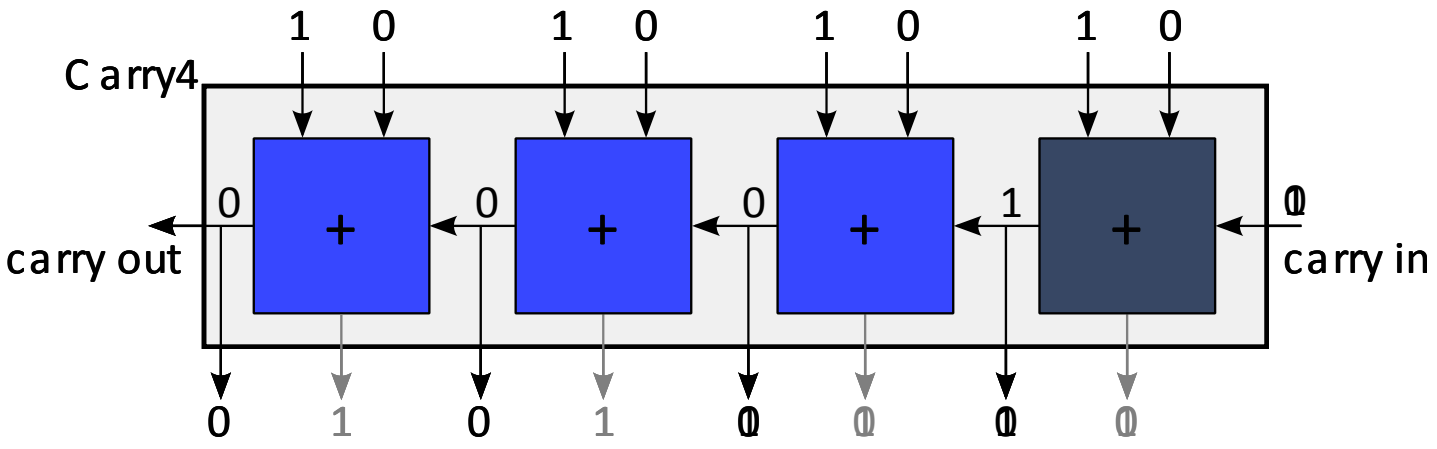

2.5
Amplitude [V]
0
Time [ns]
ANALOG DEVICES
XILINX
SPARTAN-6
255
Digital code
0
Time [ns]

# Applications



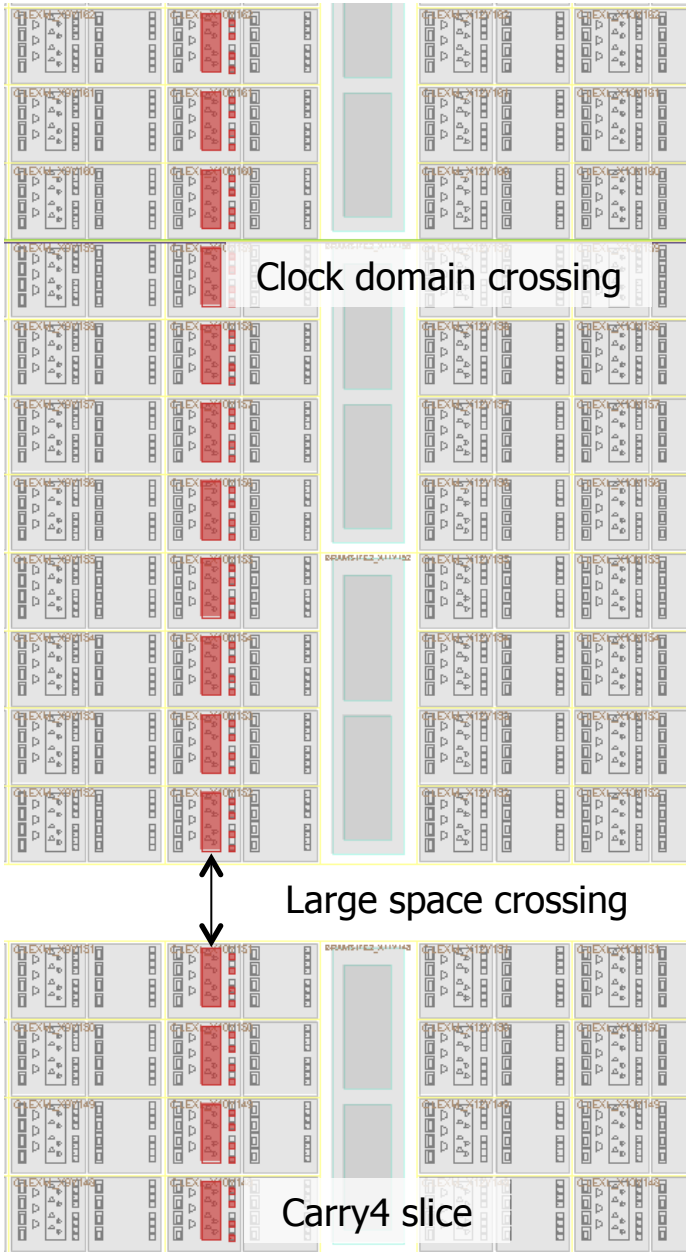
# TDC Implementation

- Carrychain (delayline) TDC
  - Propagating carry
  - Dedicated carry routing
  - Smallest delay available: ~21 ps
  - Thermometer time stamp



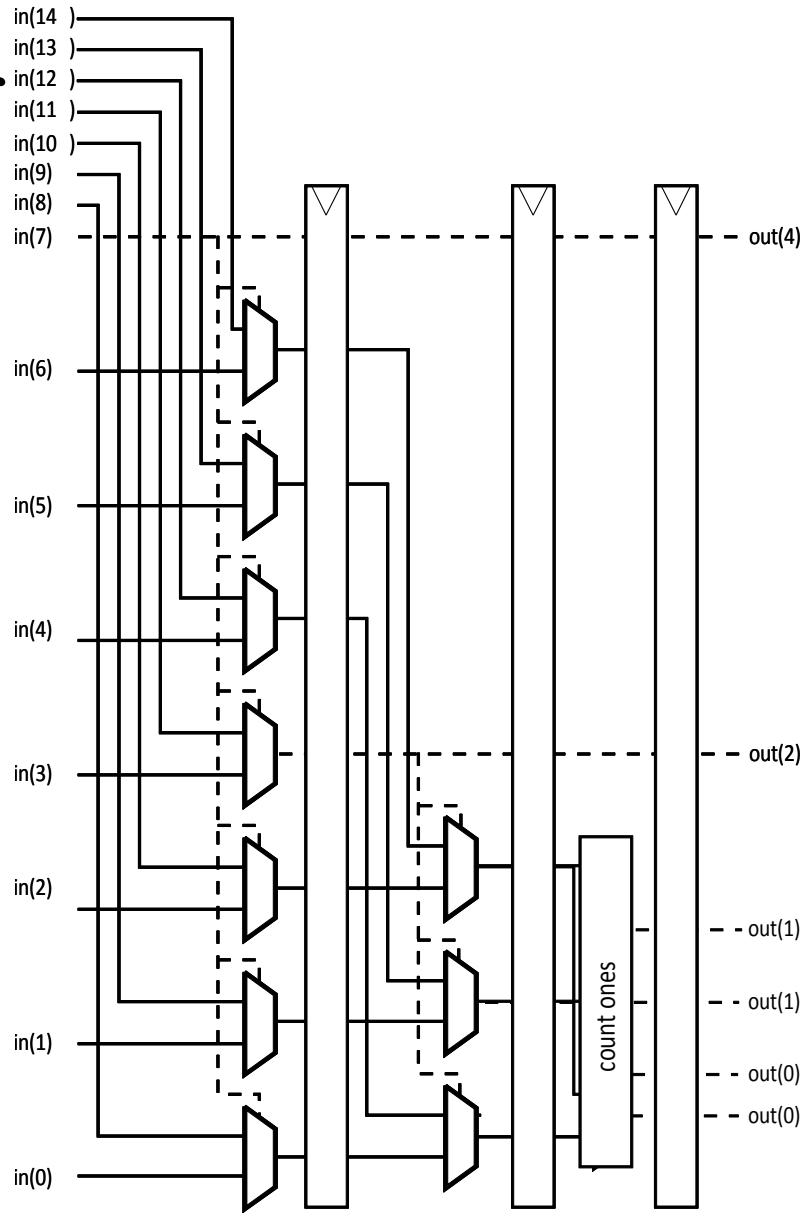
# TDC Limitations

- Carrychain (delayline) TDC
  - Performance limitations:
    - Bubbles
    - Ultra wide bins
  - Causes:
    - Carry look ahead
    - Clock
      - Domains (each 16 slices)
      - Slew / Slack
      - Setup / Hold time violations
    - Large space (each 16 slices)
    - Inter slice delay vs. Intra slice delay



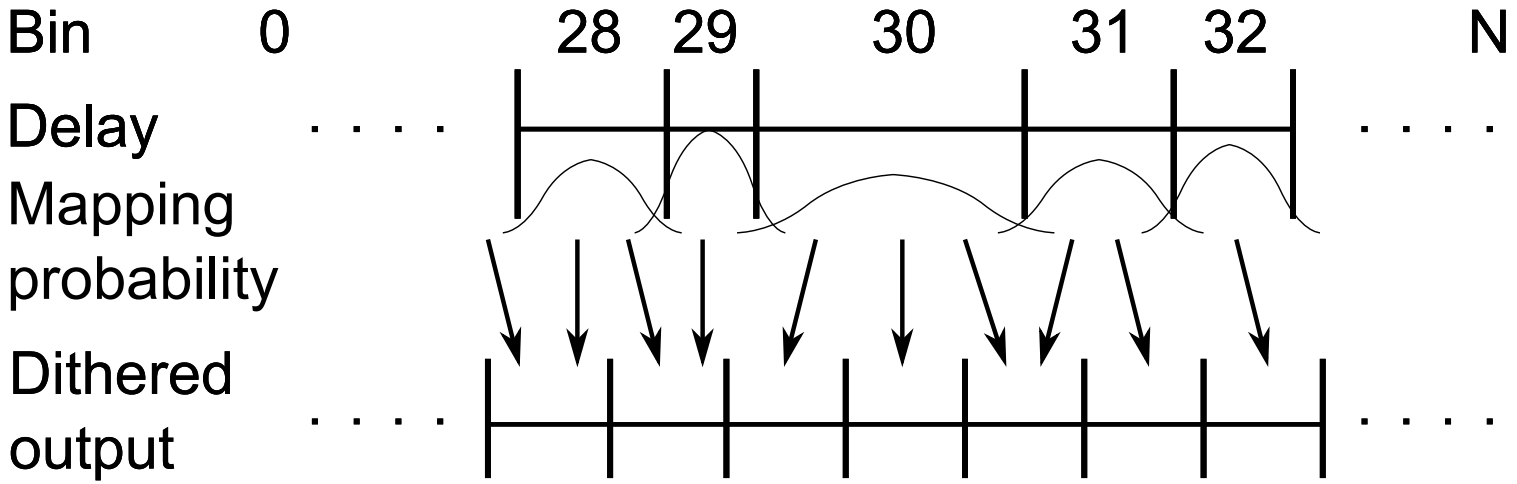
# Thermometer decoder & Bubbles

- Bubble interpretation
  - 0010111 → 4
  - 0010111 → 3
  - 0011111 → 5
- Bubble is consistent w.r.t. time
  - No correction
  - Counter on last 16 bits



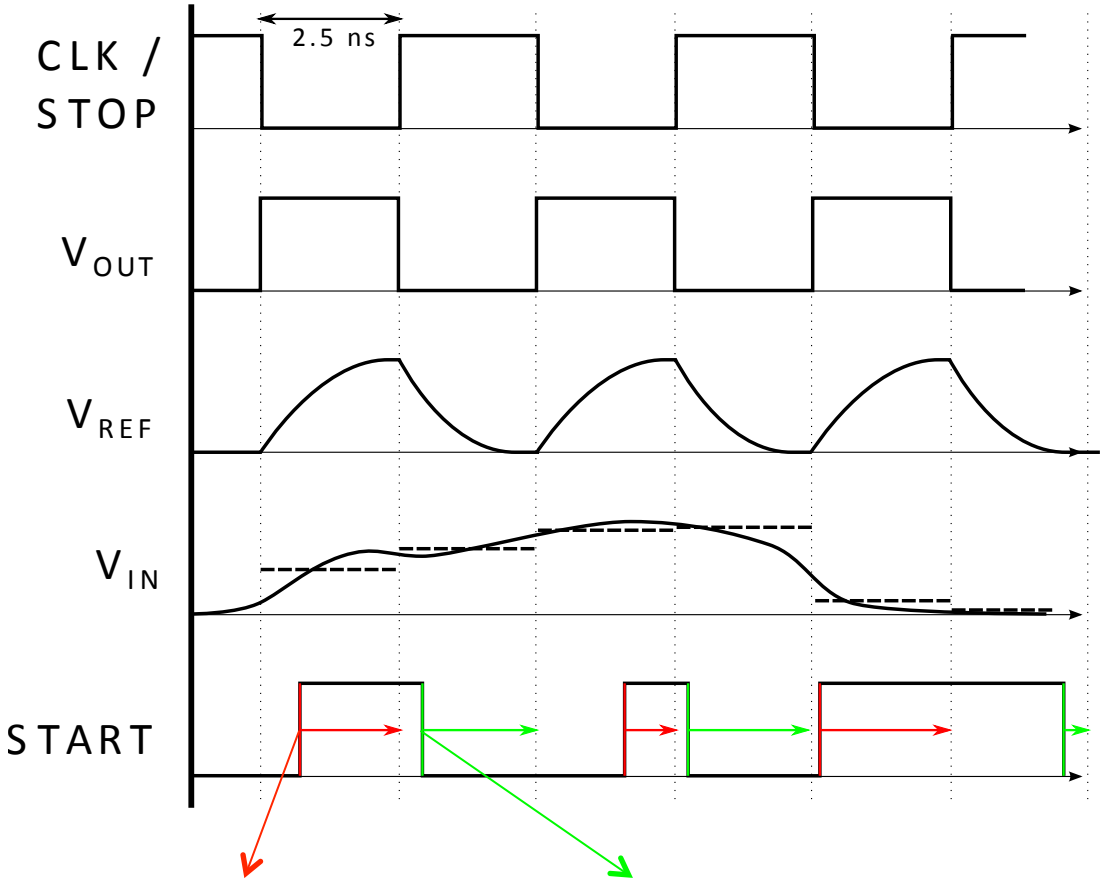
# Dithering ultra wide bins

- Dithering equalizes bin delay with a pseudo random non linear mapping on equally spaced bins
- Increase in systems linearity at expense of random noise



# 2. SYSTEM ARCHITECTURE

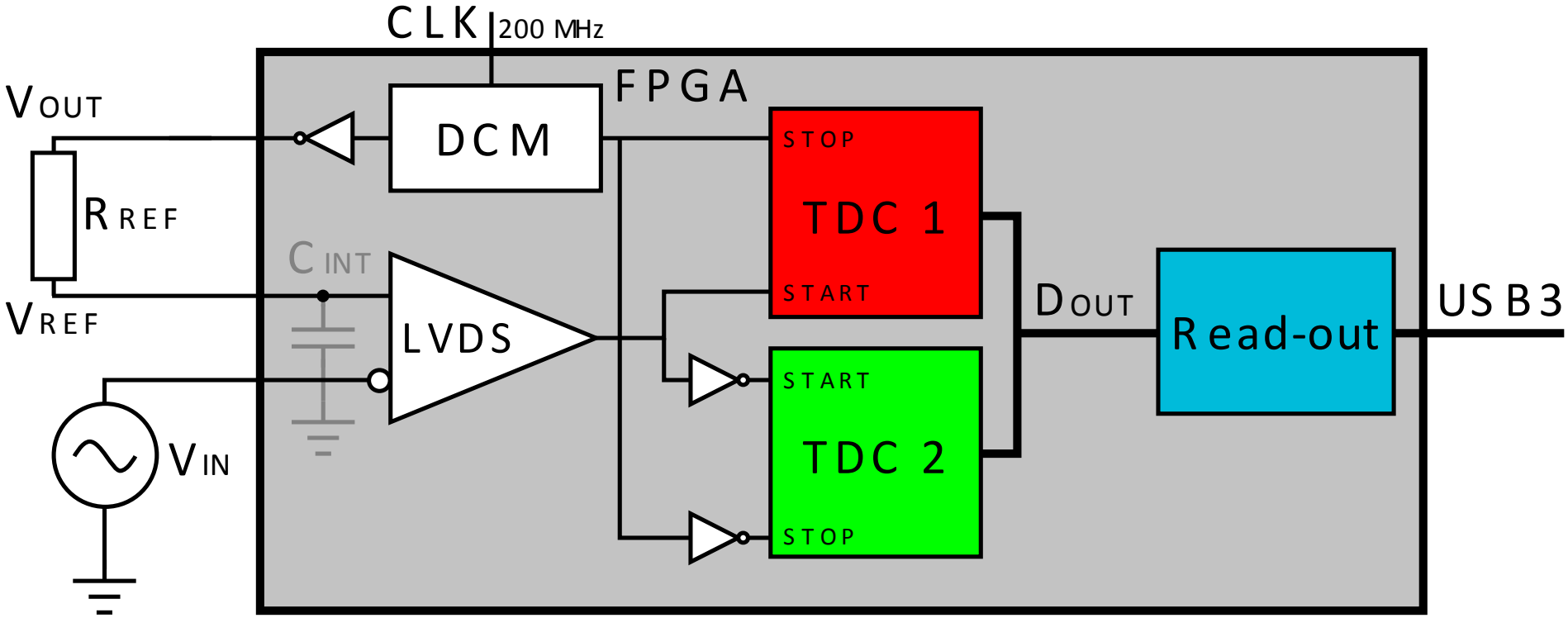
# FPGA ADC Working Principle




Positive edge timing measured with TDC 1

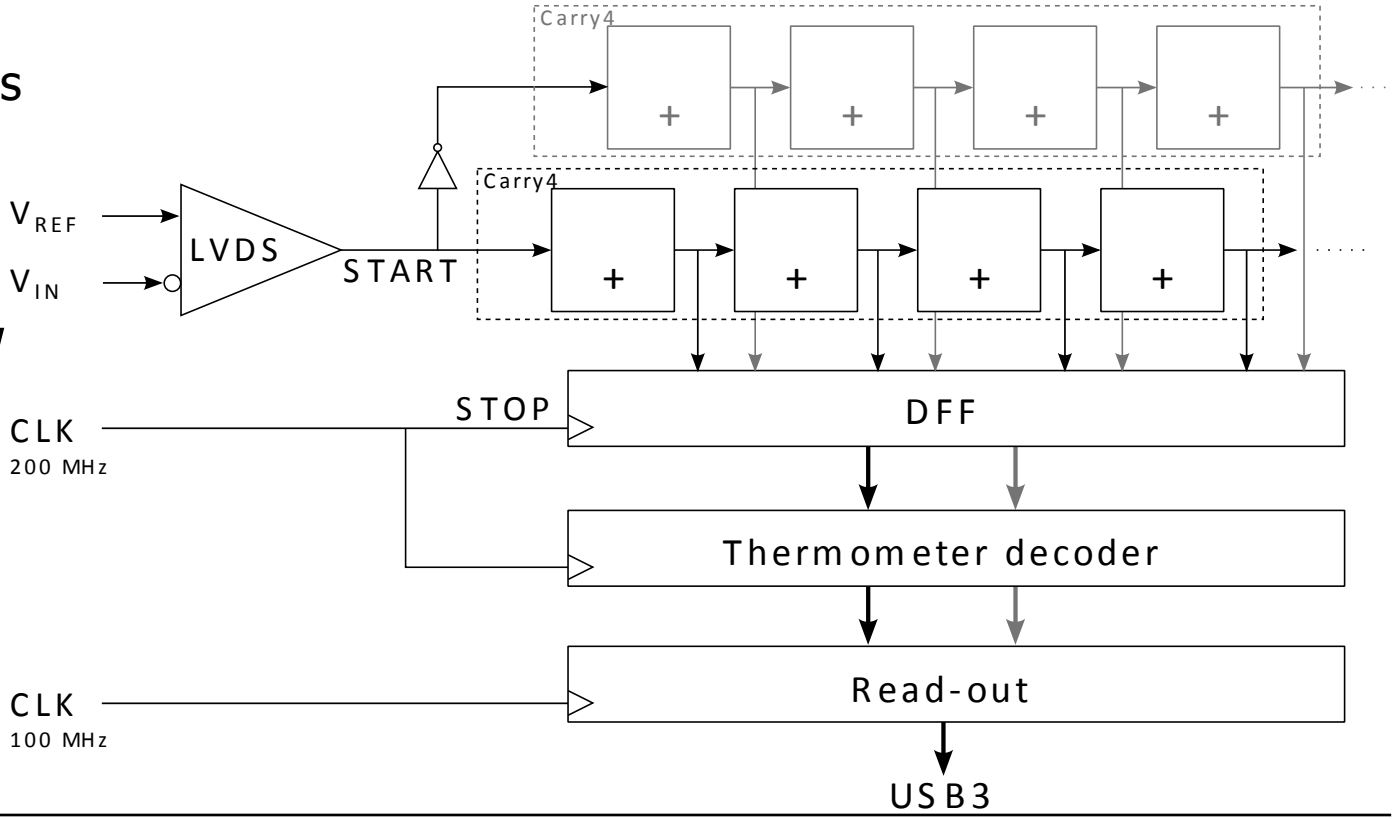
Negative edge timing measured with TDC 2

# Reference ramp



# System & TDCs

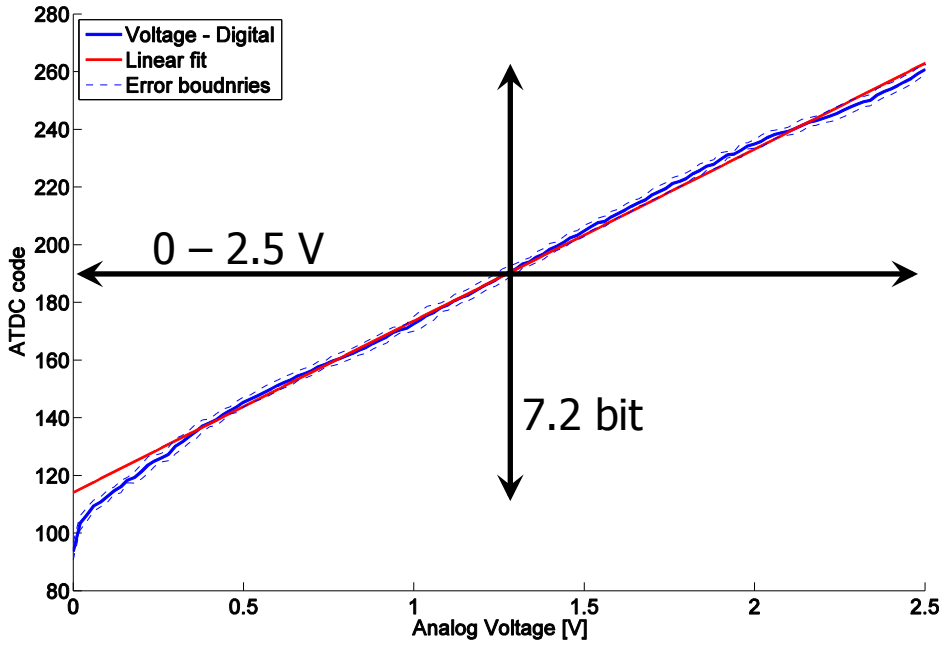
- 2 carrychains TDC
  - 200 MHz
  - 128 adders
  - 32 slices
- Total slices < 400
- P = 410 mW



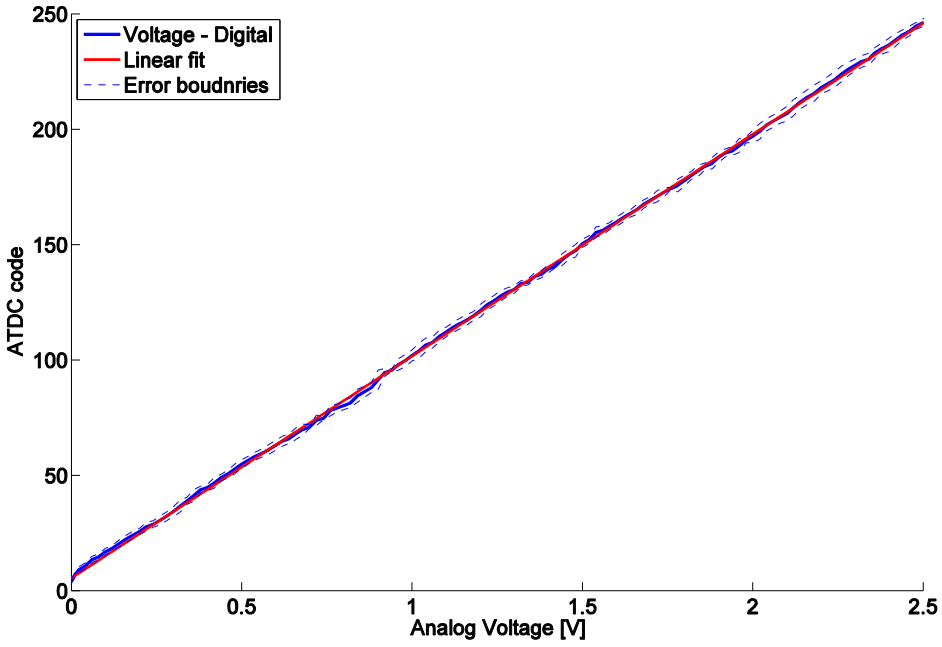
# 3. RESULTS

# Transfer curve

Resolution (LSB) = 17 mV

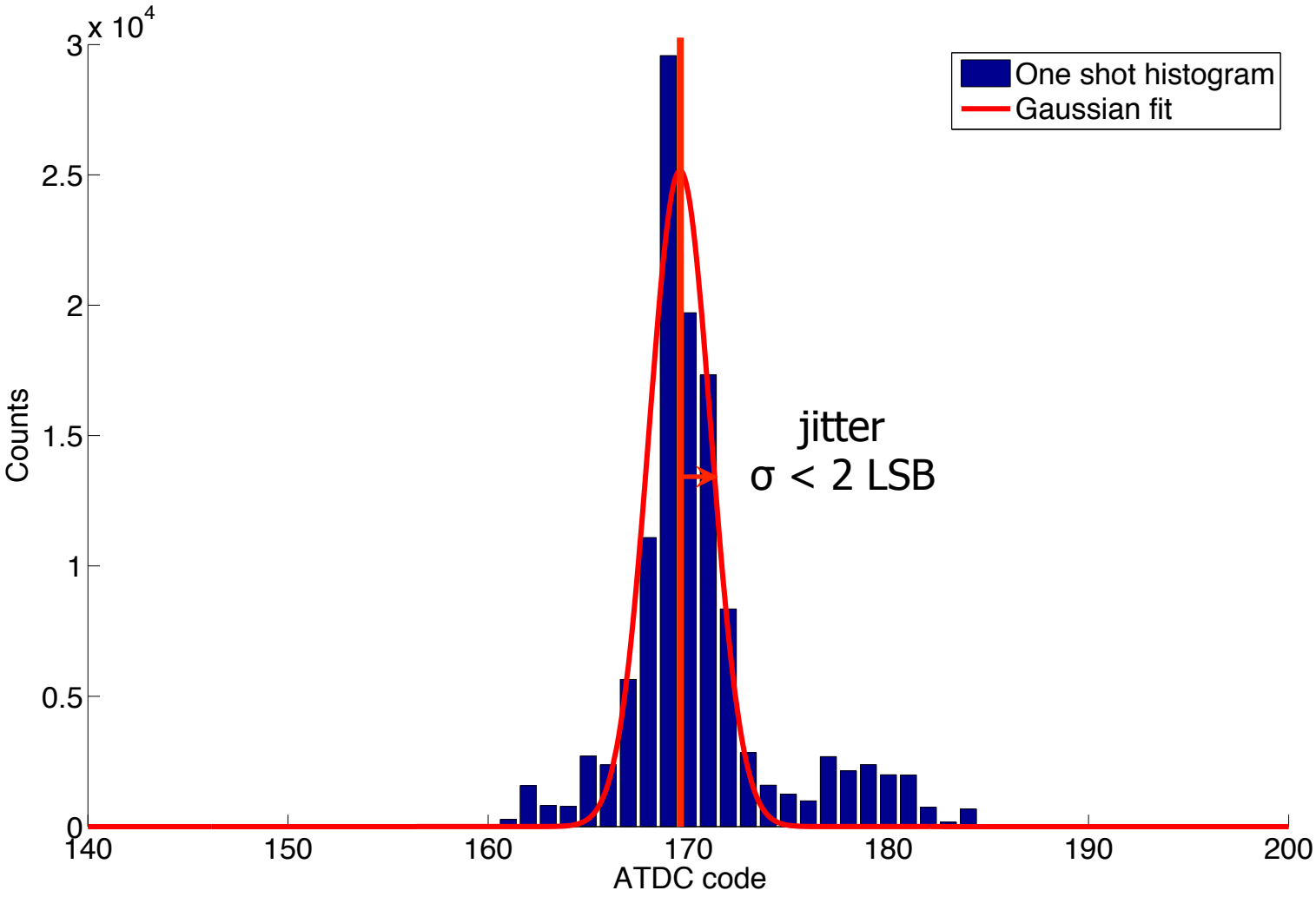



Before calibration



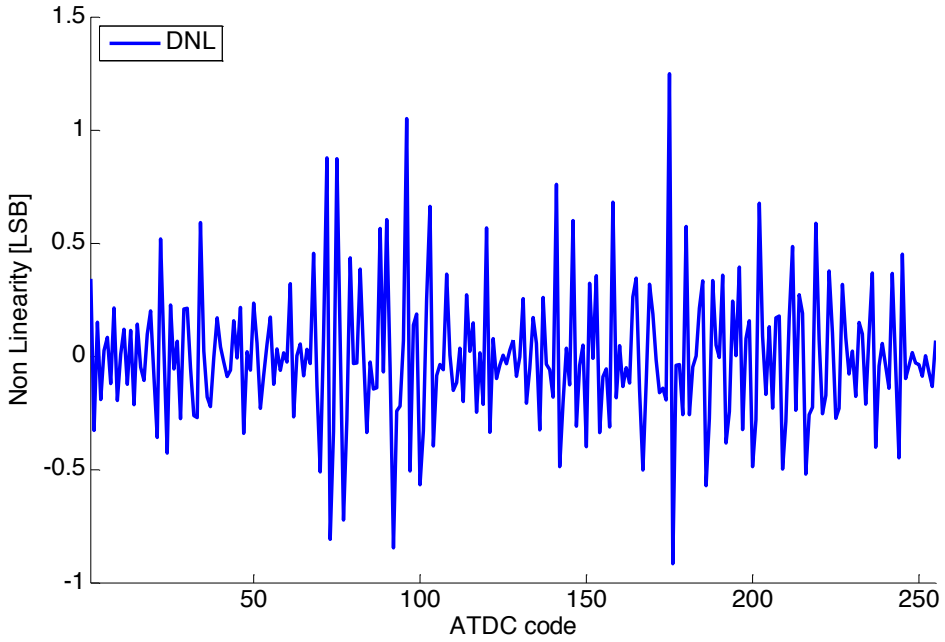

After calibration

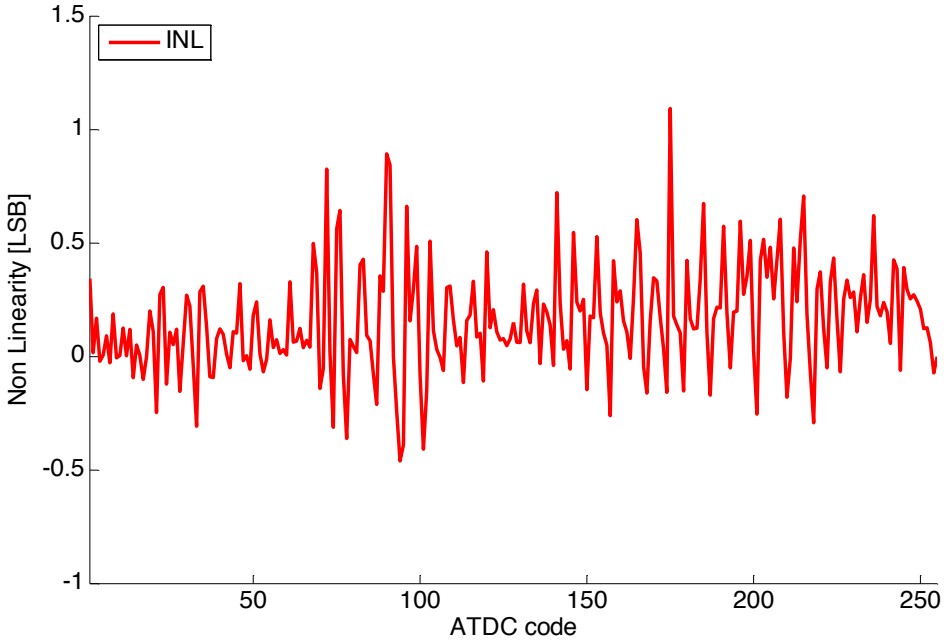
# DC measurement (single shot)



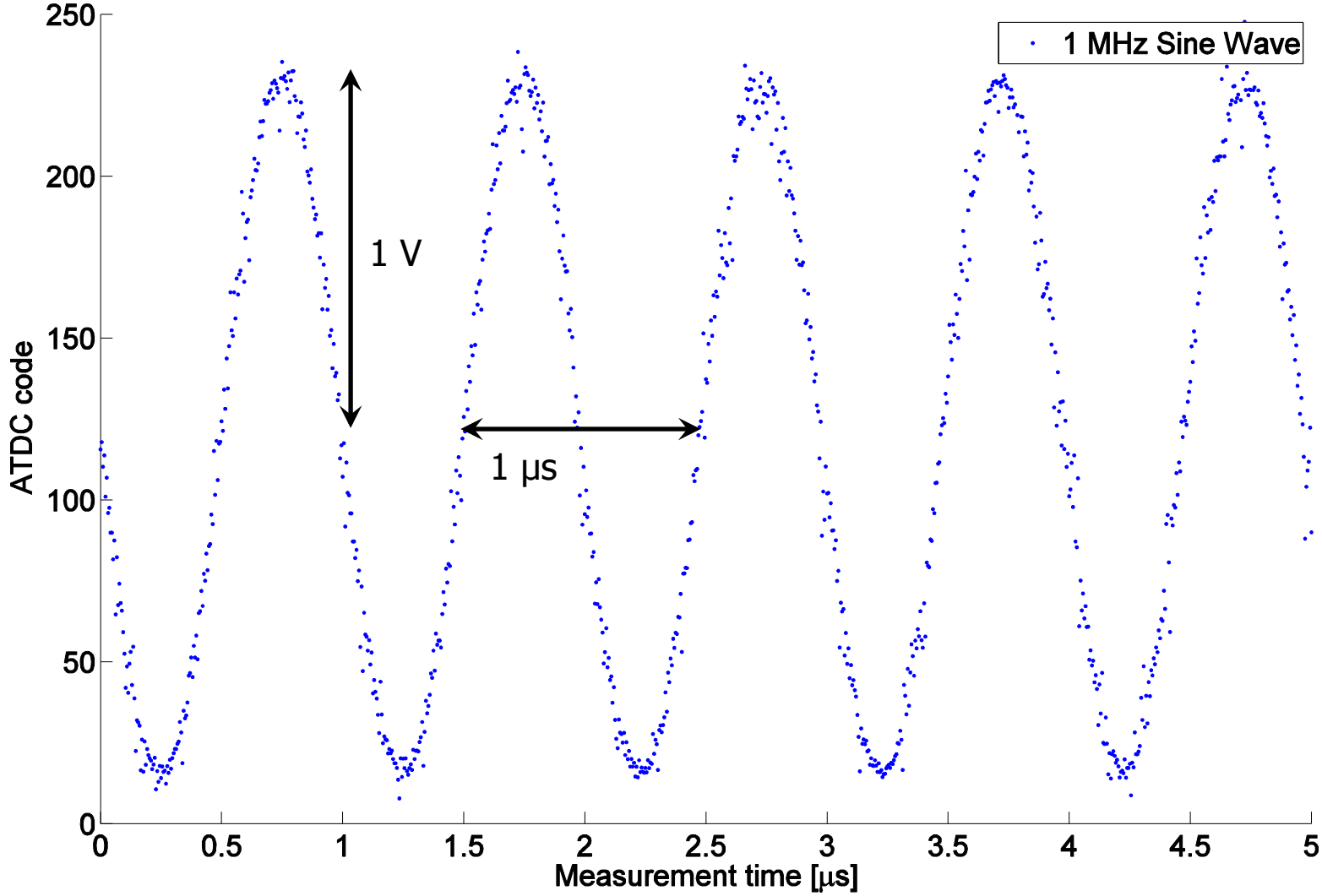
# Non linearities – DNL/INL

- DNL [-0.9 1.3] LSB
- INL [-0.5 1.1] LSB

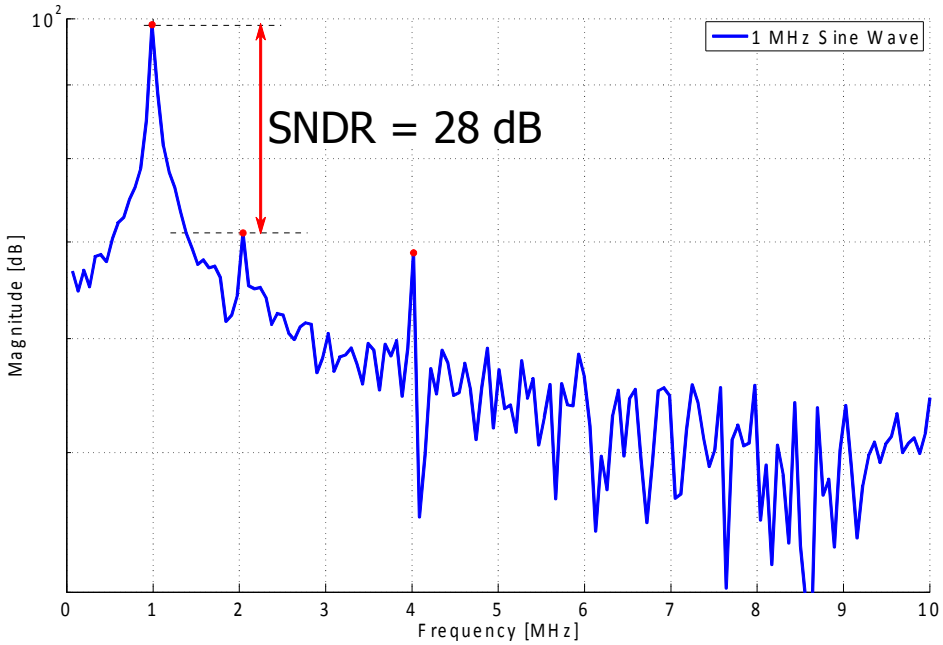


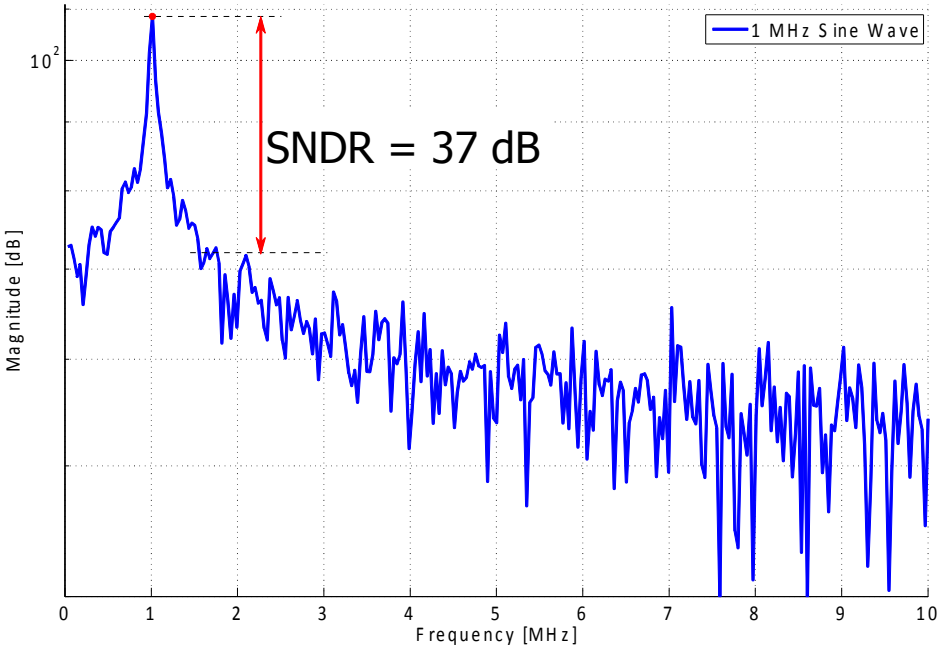
# AC measurement – Time Domain



# AC measurement – Frequency Domain




Before calibration

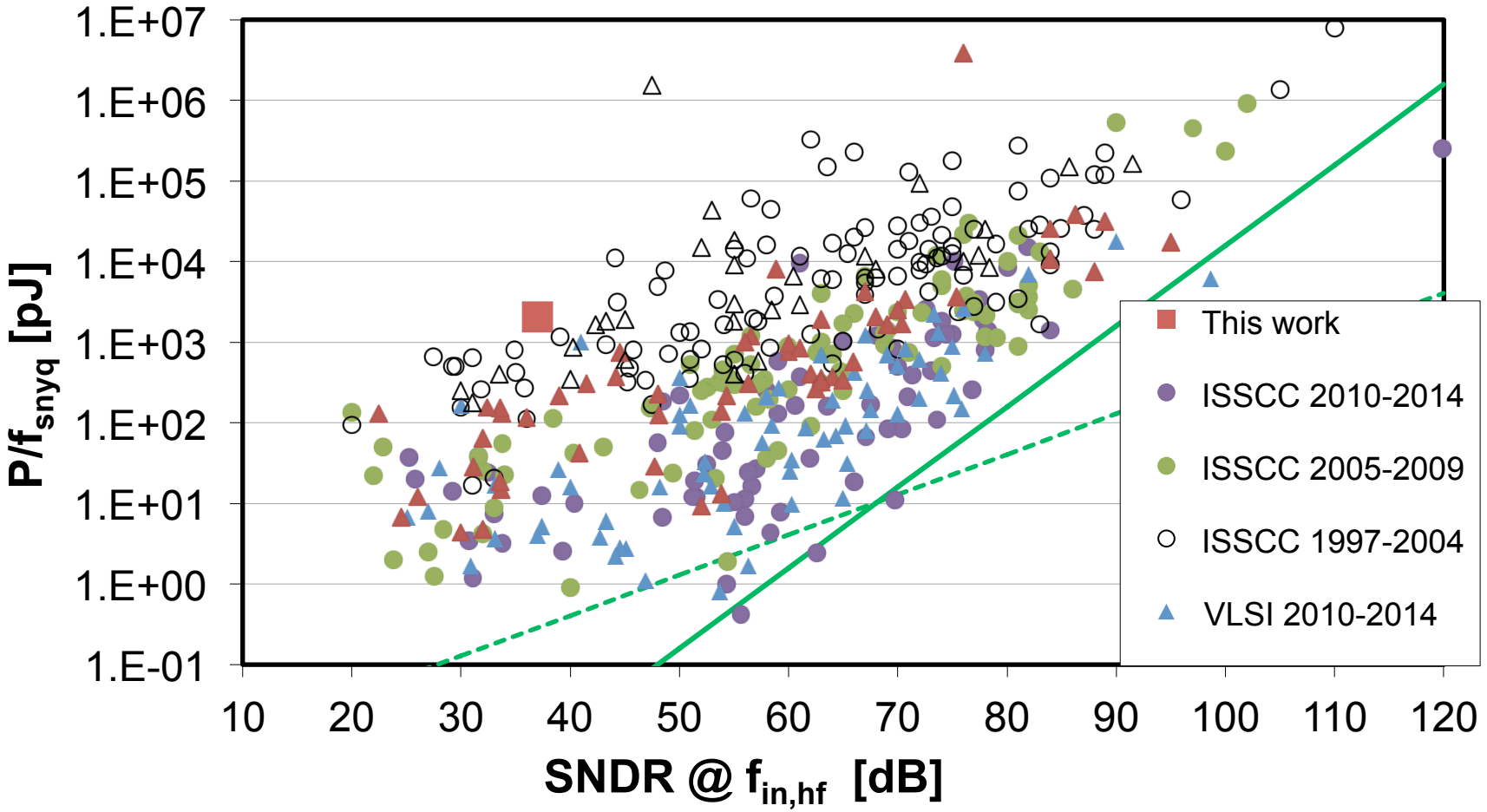



After calibration

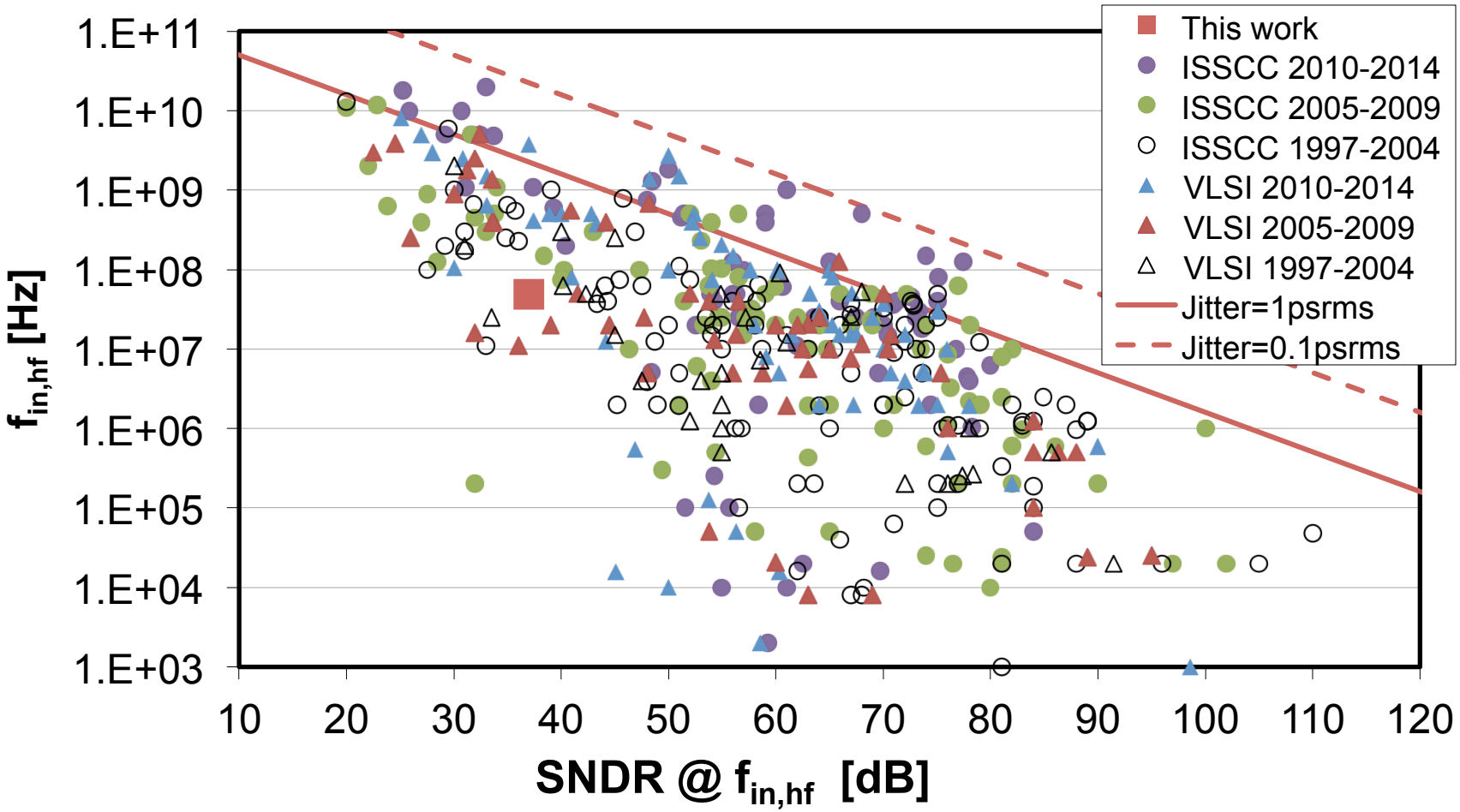
# Comparison with other FPGA ADCs

| | Carrychain TDC | Clock phase TDC [7] | Delta Sigma Modulator [5,6] | XADC [10] |
|---|---|---|---|---|
| **Clock speed [MHz]** | 200 | 360 | 100 | |
| **Conversion speed [MS/s]** | 200 | 22.5 | 0.5 to 0.05 | 1 |
| **Voltage range [V]** | 0 – 2.5 | 0 – 3.3 | 0 – 3.3 | 0 – 1.0 |
| **Digital range** | 7.2 bit | 6 bit | 10 bit to 16 bit | 12 bit |
| **ENOB** | 6 bit | | 9 bit | 10 bit |
| **Resolution [mV]** | 17 | 52 | 3 | 0.25 |
| **DNL [LSB]** | [-0.9 1.3] | | | ± 1 |
| **INL [LSB]** | [-0.5 1.1] | | | ± 2 |
| **Error σ [LSB]** | 2 | | | 1 |
| **External components** | 1 | 4 | 2 - 3 | 0 |

# Comparison with ASIC – Murmann survey
# Conversion energy vs. SNDR



# Comparison with ASIC – Murmann survey
# Signal frequency vs. SNDR



# 4. CONCLUSION

# Conclusion

- Best performing FPGA ADC implemented with 200 MS/s, 6 bits of ENOB and a high linearity.
  - 10×higher sampling rate with 1 bit higher resolution (compared to clock phase TDC based ADC)
  - 200×higher sampling rate with 4 bits lower resolution (compared to Xilinx XADC: found in Xilinx 7 series FPGAs)
  - FPGA ADC can compete with somewhat older ASIC ADCs
- Next steps:
  - 1 GS/s ADC
  - Auto calibration
  - Multichannel
  - DAC

# VHDL Source – Available online


http://cas.tudelft.nl/fpga_tdc