



# 200 MS/s ADC implemented in a FPGA employing TDCs

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15 April 2015

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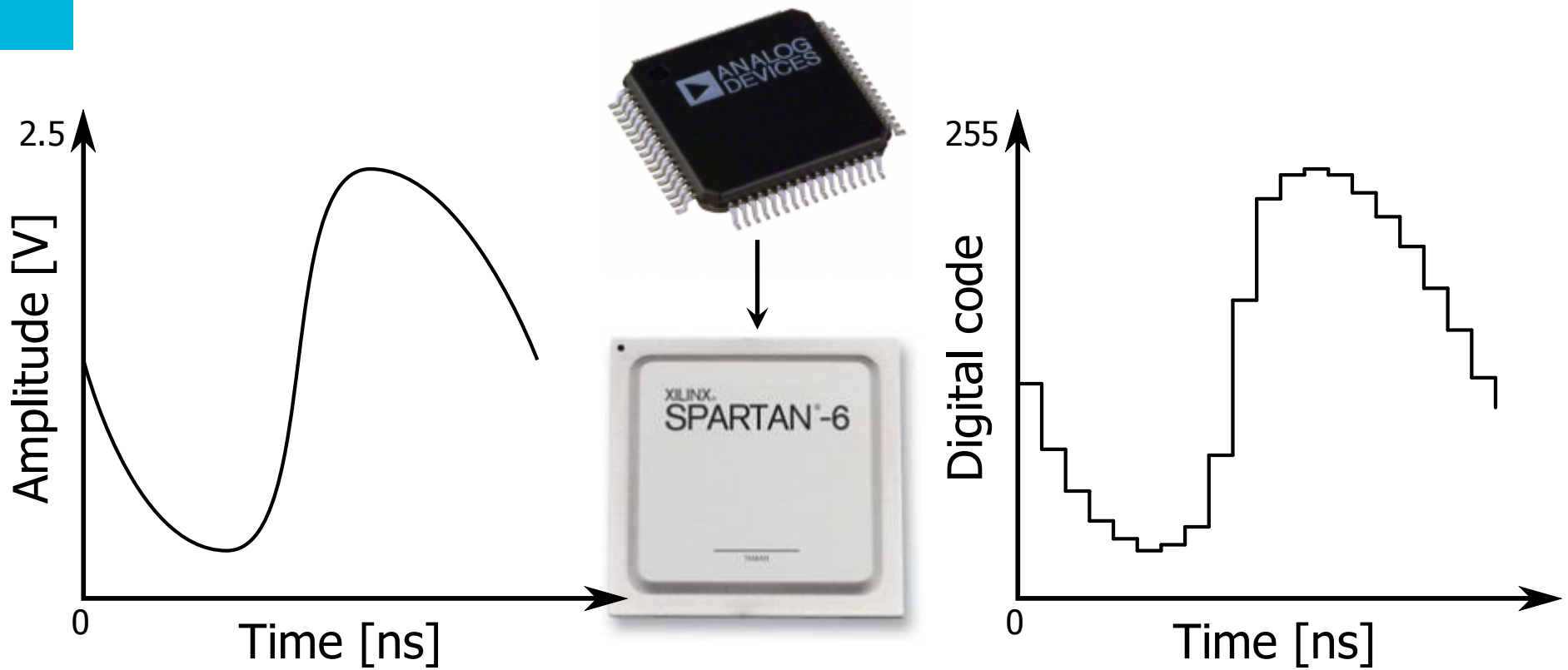


## Developing FPGA ADCs

- Introduction
- System Architecture
- Results
- Conclusion

# 1. INTRODUCTION

# FPGA ADCs?



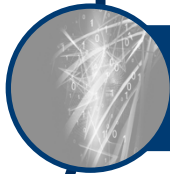
# Applications



Sensor networks



Industrial control systems



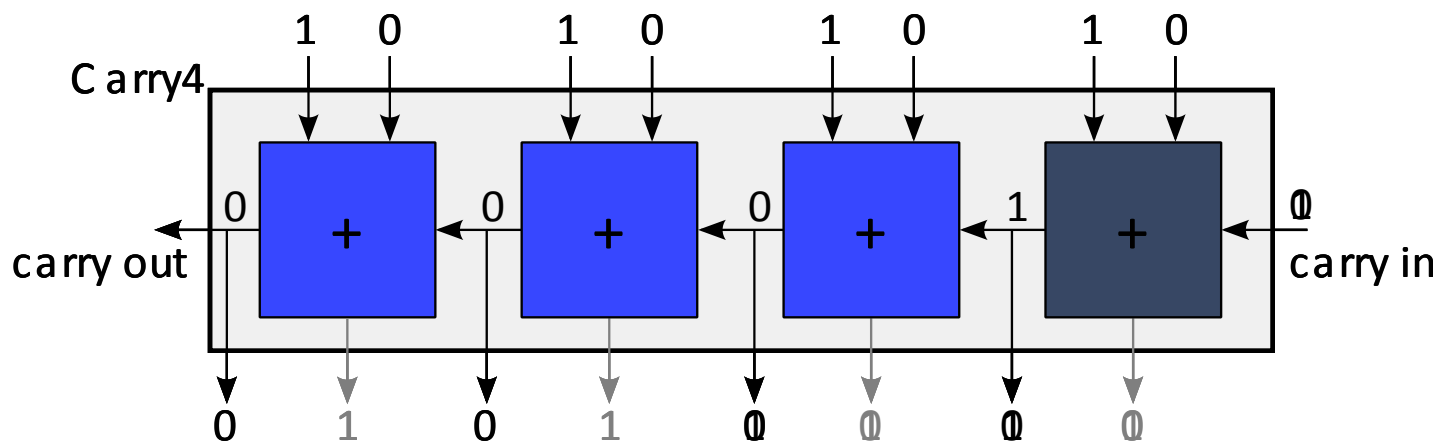
Physics experiments



Medical electronics

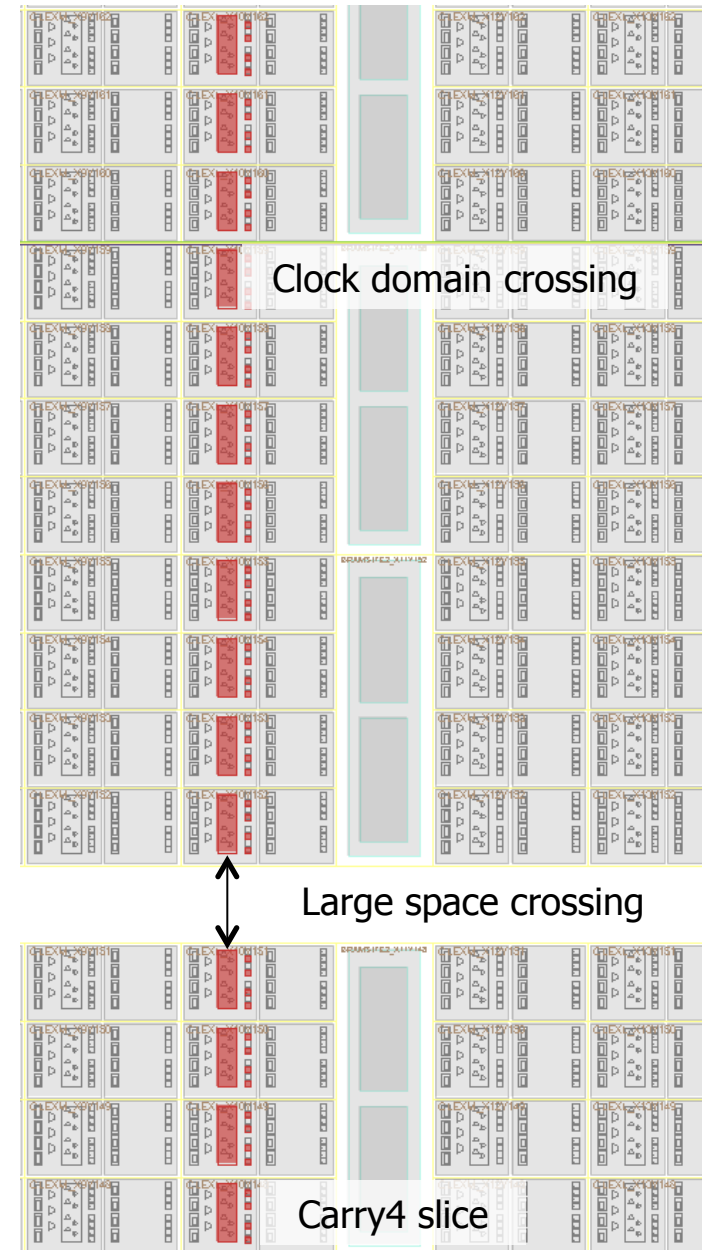
# TDC Implementation

- Carrychain (delayline) TDC
  - Propagating carry
  - Dedicated carry routing
  - Smallest delay available: ~21 ps
  - Thermometer time stamp



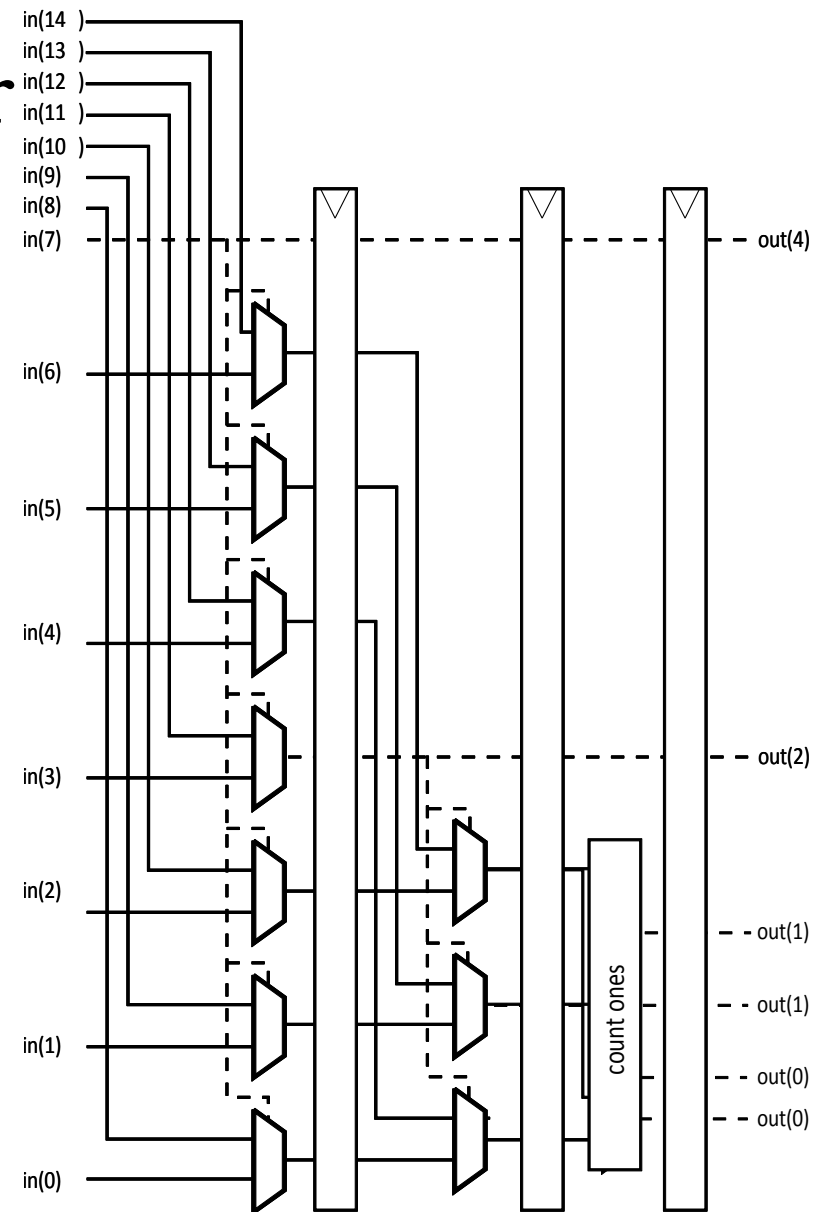
# TDC Limitations

- Carrychain (delayline) TDC
  - Performance limitations:
    - Bubbles
    - Ultra wide bins
  - Causes:
    - Carry look ahead
    - Clock
      - Domains (each 16 slices)
      - Slew / Slack
      - Setup / Hold time violations
    - Large space (each 16 slices)
    - Inter slice delay vs. Intra slice delay



# Thermometer decoder & Bubbles

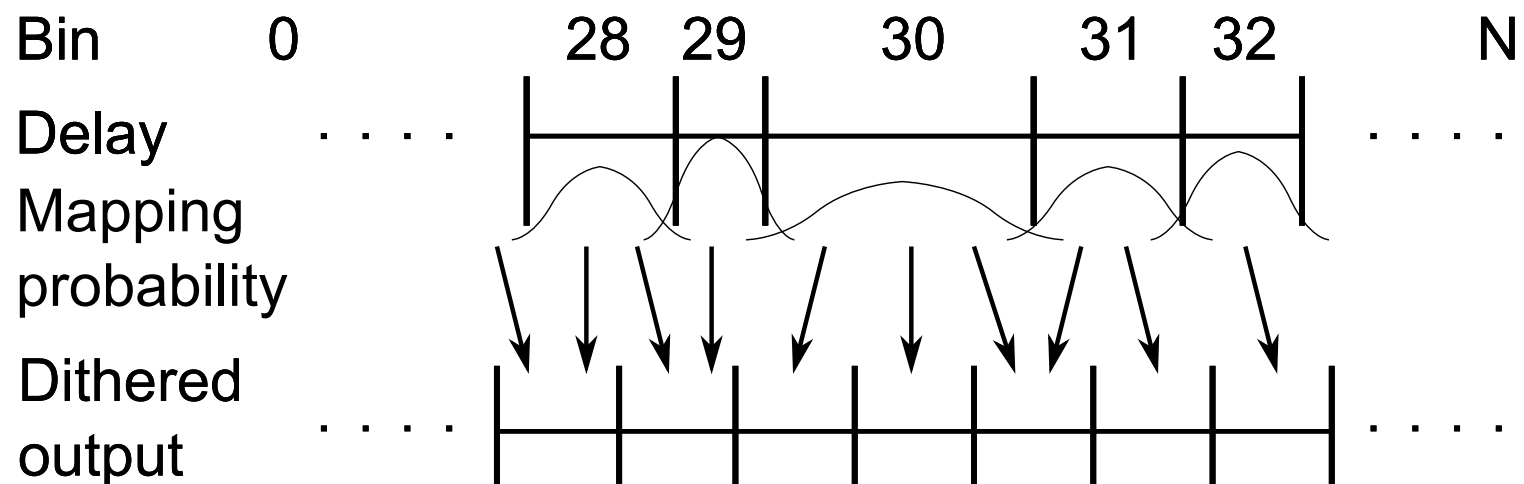
- Bubble interpretation
  - 0010111  $\rightarrow$  4
  - 0010111  $\rightarrow$  3
  - 0011111  $\rightarrow$  5
- Bubble is consistent w.r.t. time
  - No correction
  - Counter on last 16 bits





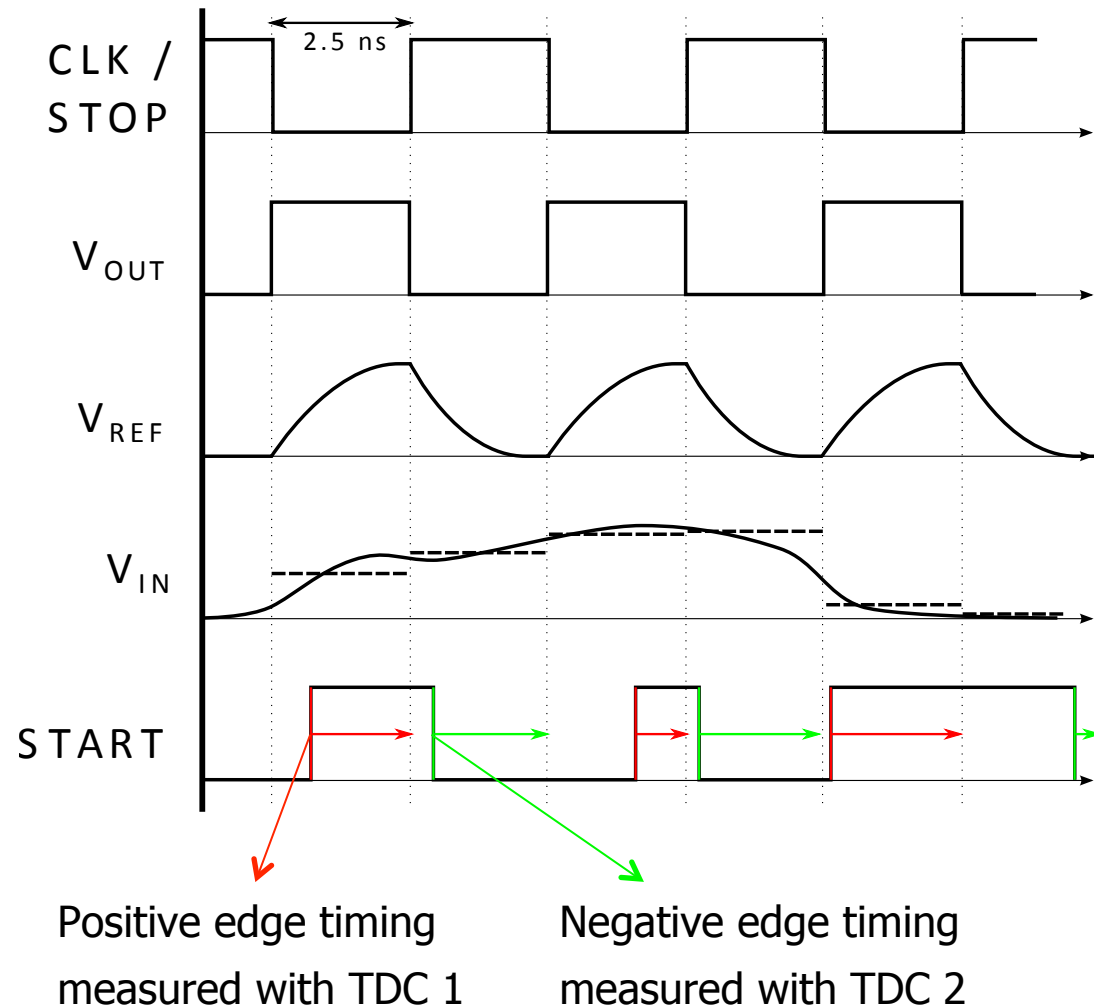
# Dithering ultra wide bins

- Dithering equalizes bin delay with a pseudo random non linear mapping on equally spaced bins
- Increase in systems linearity at expense of random noise

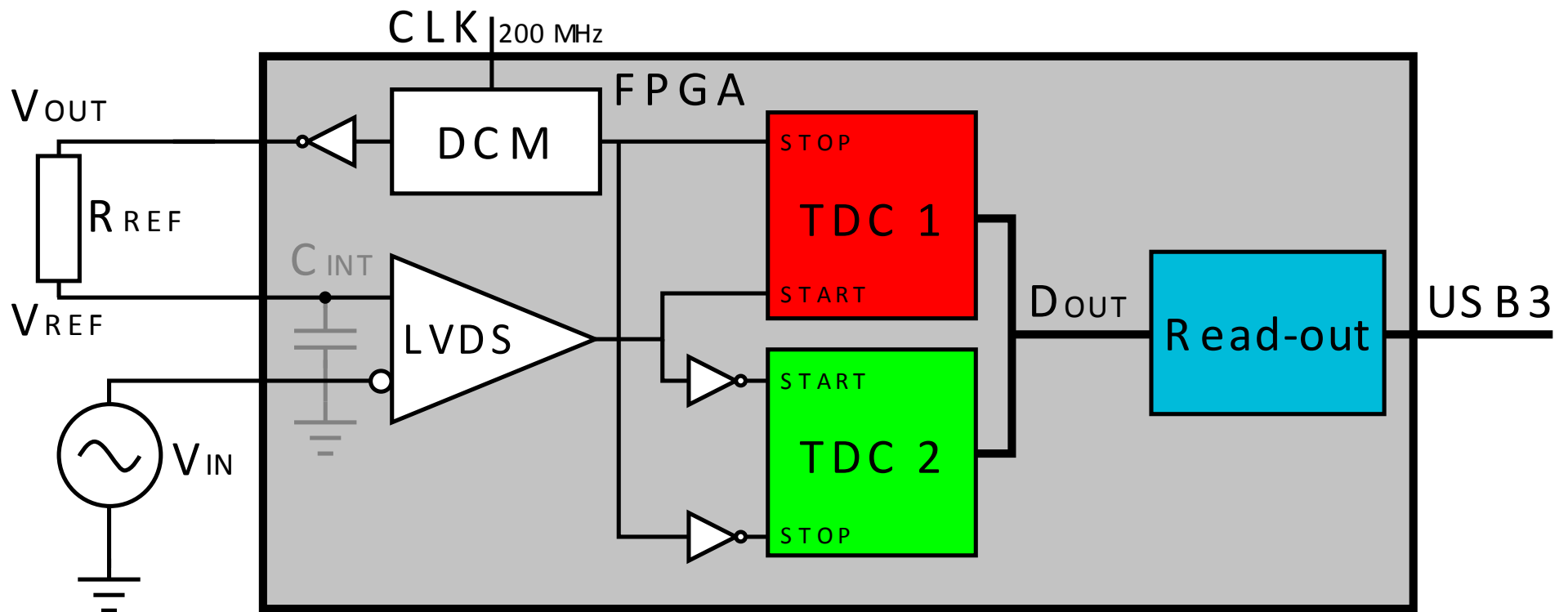


# 2. SYSTEM ARCHITECTURE

# FPGA ADC Working Principle

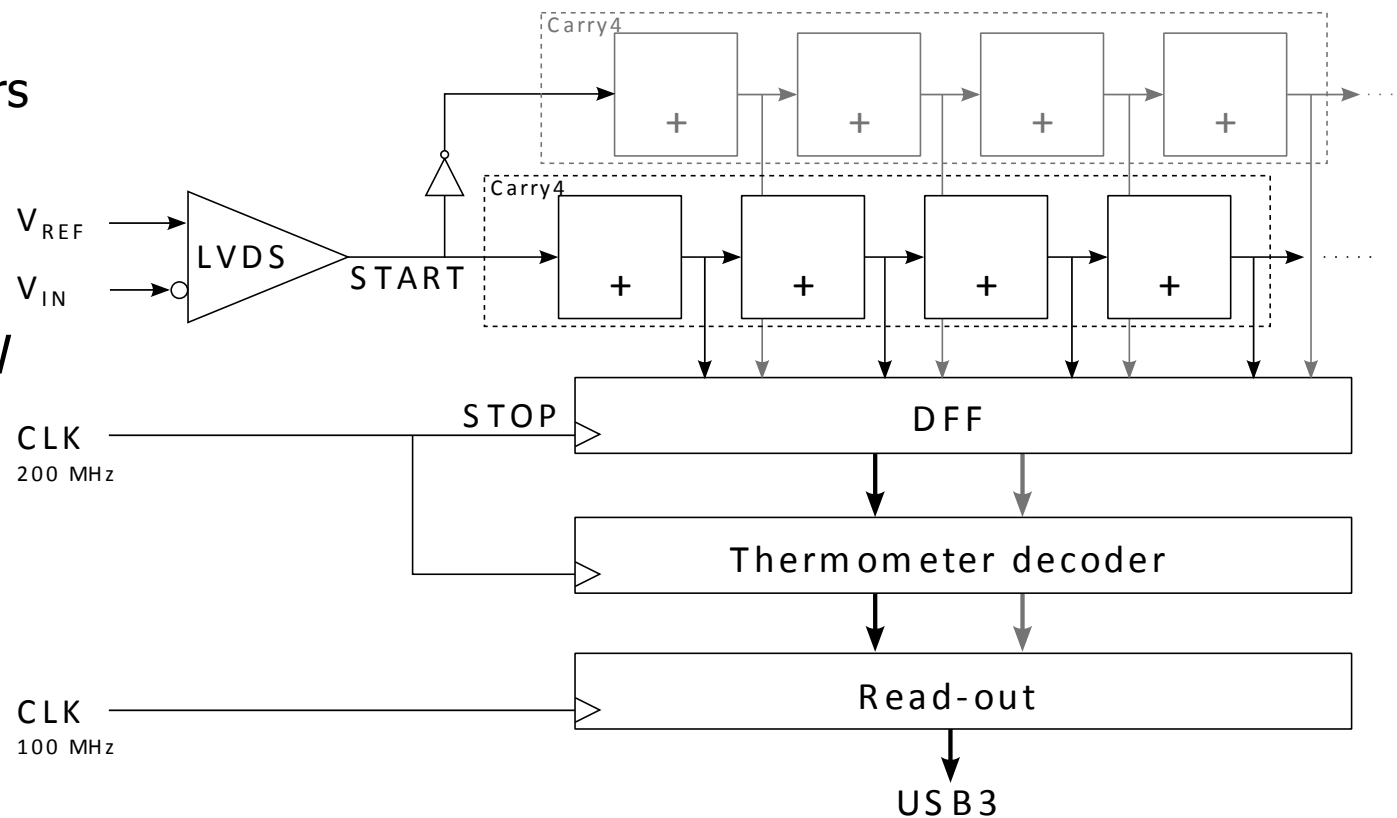


# Reference ramp



# System & TDCs

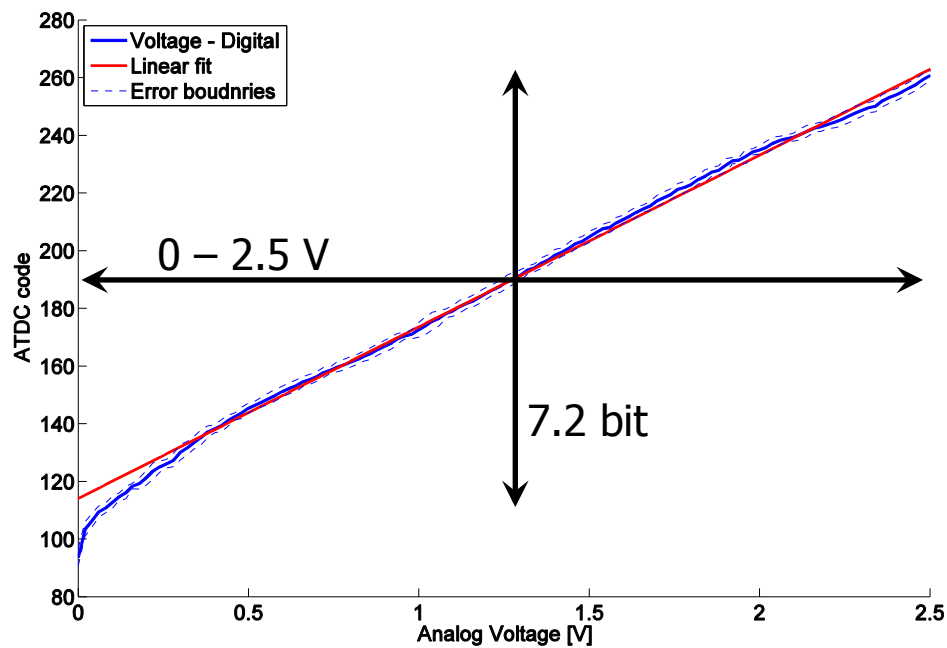
- 2 carrychains TDC
  - 200 MHz
  - 128 adders
  - 32 slices
- Total slices < 400
- P = 410 mW



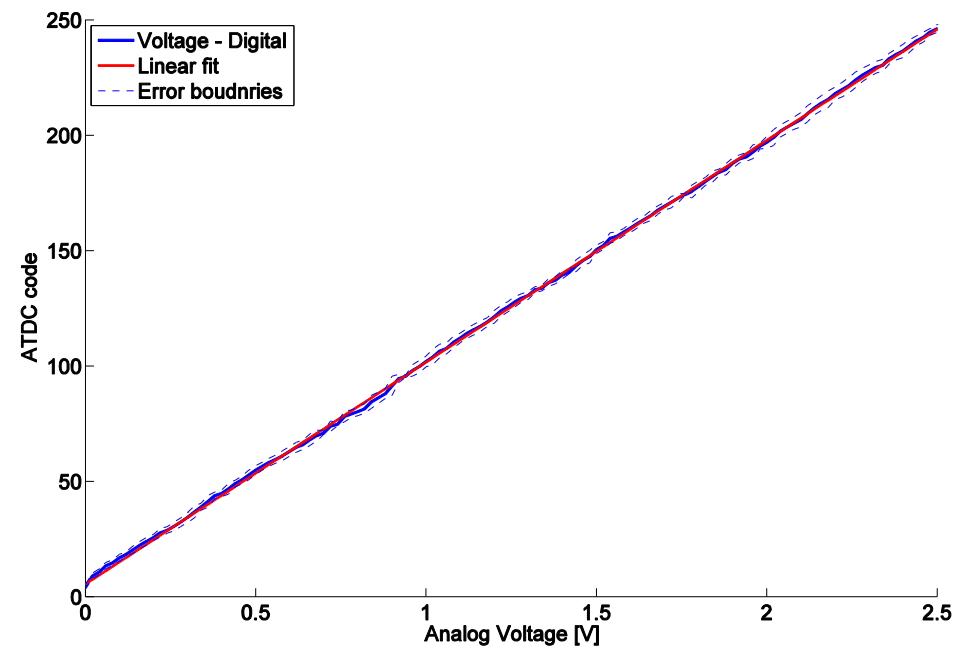
# 3. RESULTS

# Transfer curve

Resolution (LSB) = 17 mV

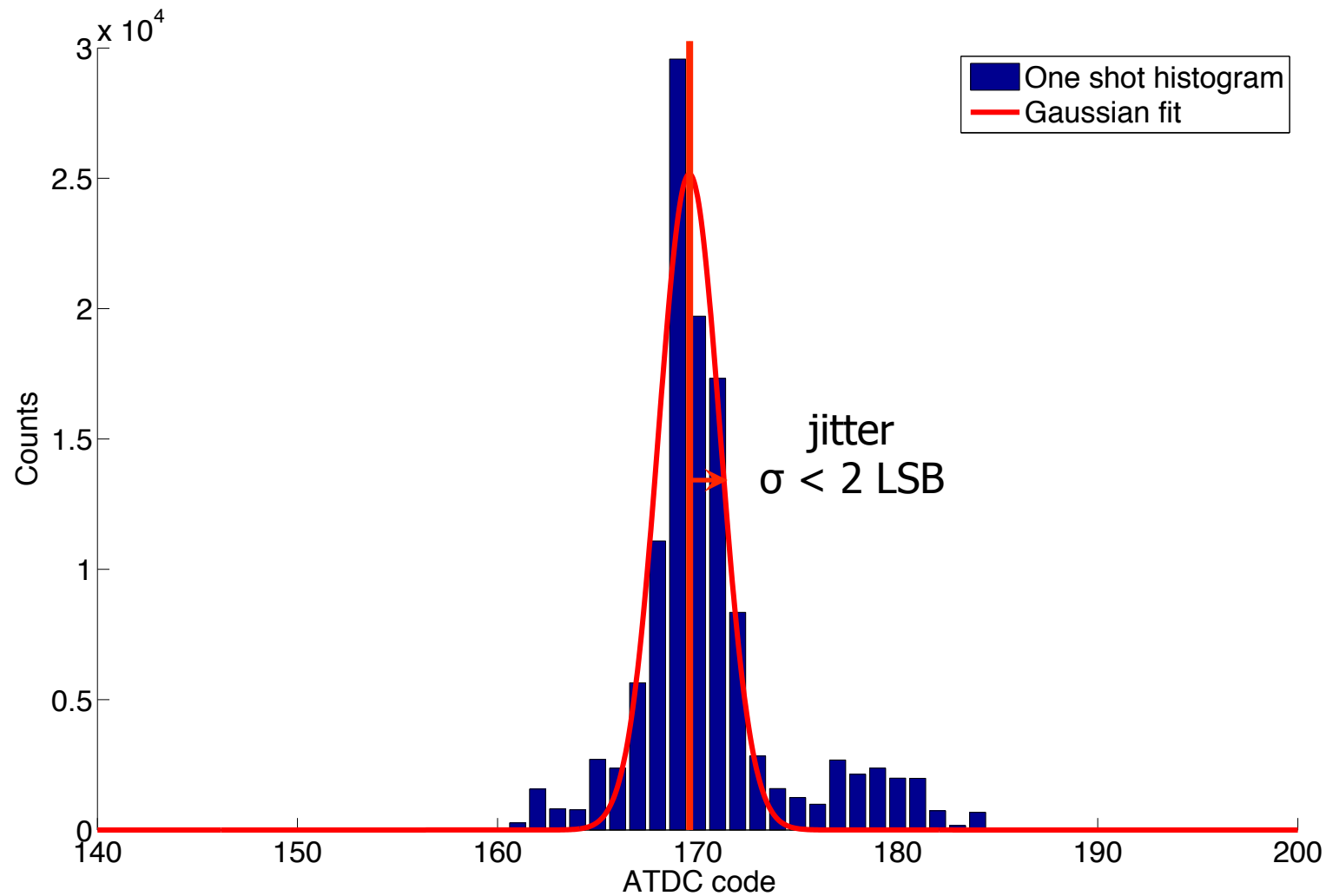


Before calibration



After calibration

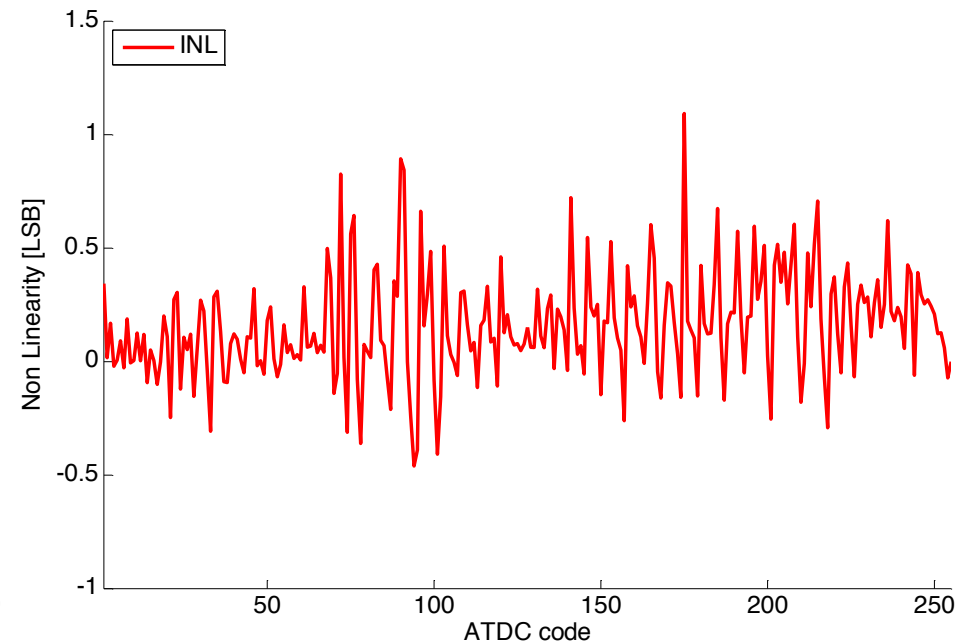
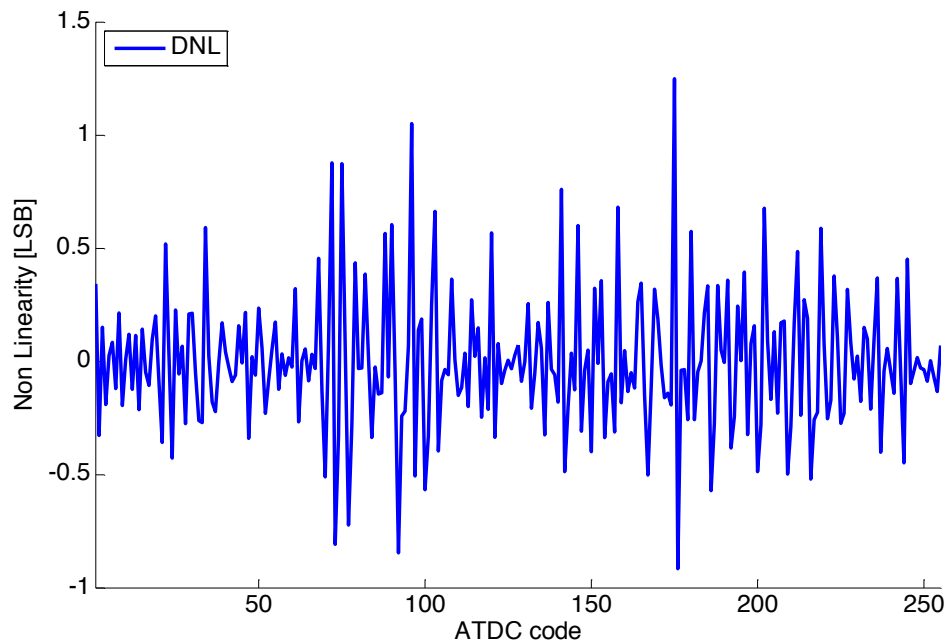
# DC measurement (single shot)



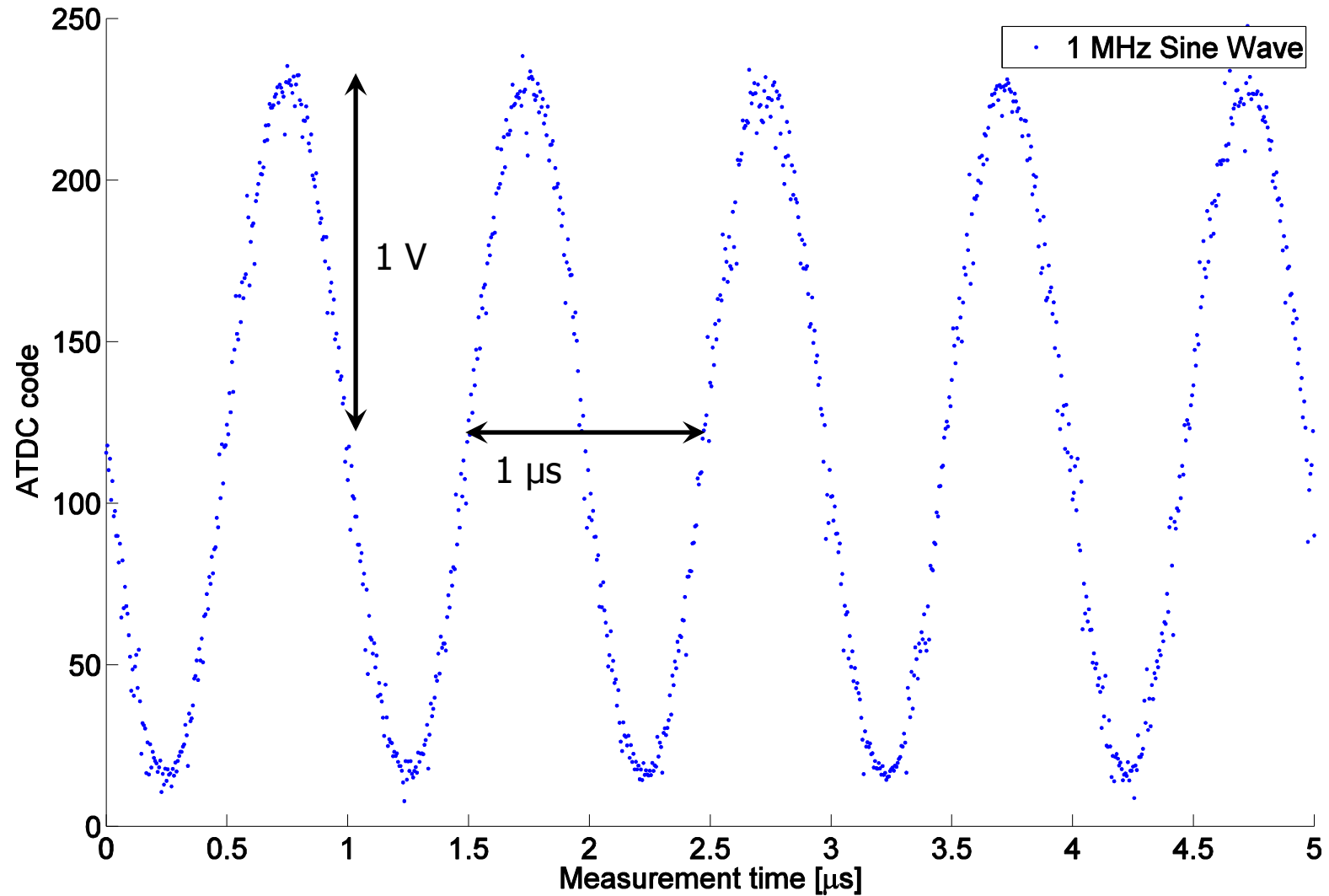


# Non linearities – DNL/INL

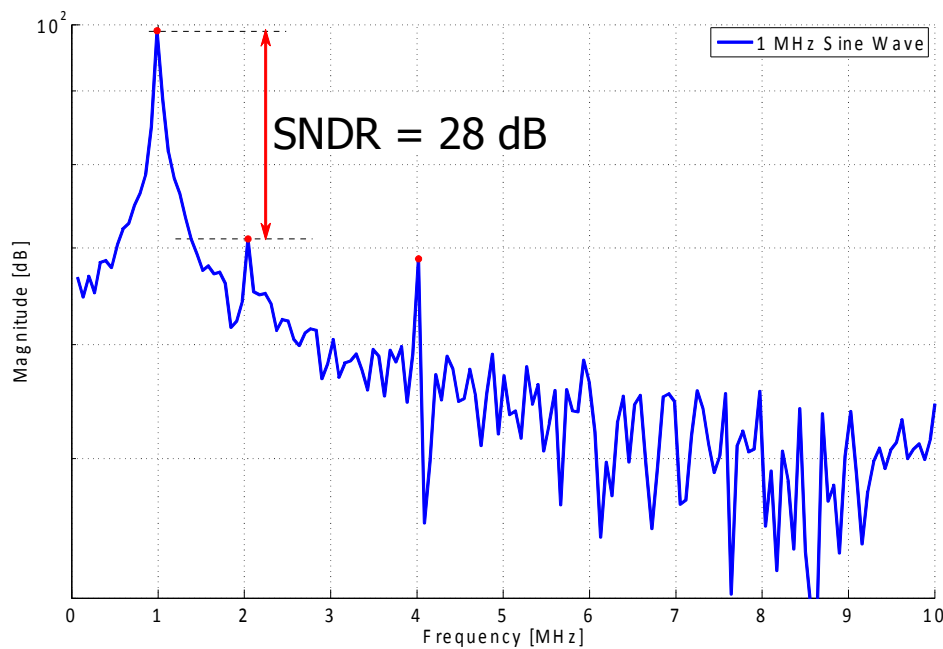
- DNL [-0.9 1.3] LSB
- INL [-0.5 1.1] LSB



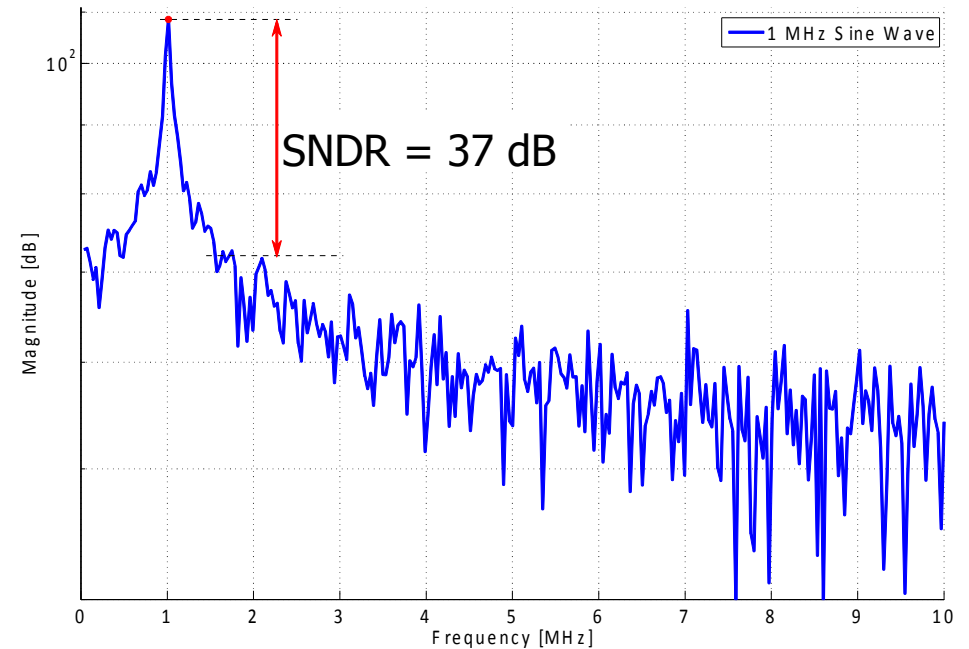
# AC measurement – Time Domain



# AC measurement – Frequency Domain



Before calibration



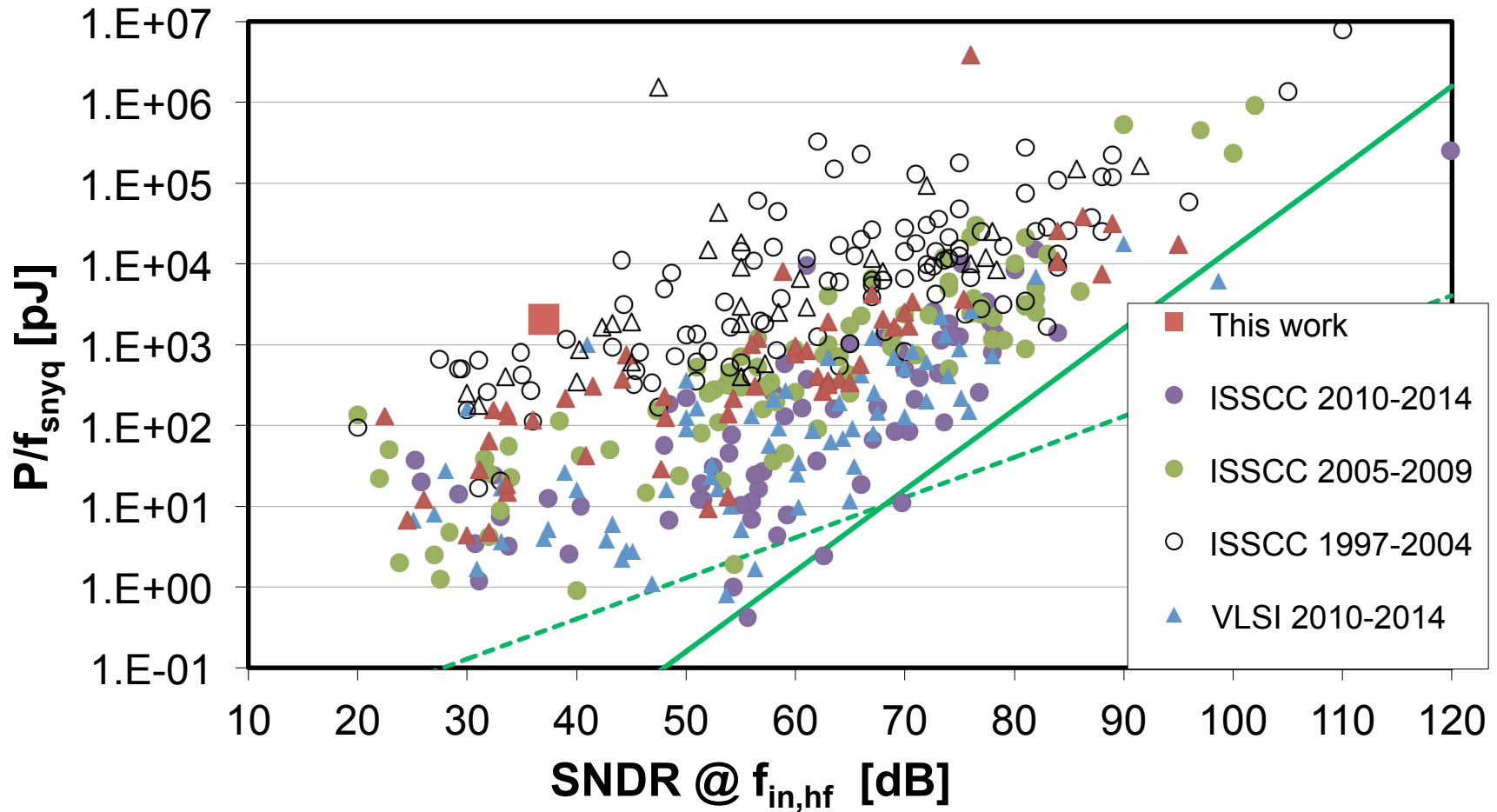
After calibration

# Comparison with other FPGA ADCs

	Carrychain TDC	Clock phase TDC [7]	Delta Sigma Modulator [5,6]	XADC [10]
Clock speed [MHz]	200	360	100	
Conversion speed [MS/s]	200	22.5	0.5 to 0.05	1
Voltage range [V]	0 – 2.5	0 – 3.3	0 – 3.3	0 – 1.0
Digital range	7.2 bit	6 bit	10 bit to 16 bit	12 bit
ENOB	6 bit		9 bit	10 bit
Resolution [mV]	17	52	3	0.25
DNL [LSB]	[-0.9 1.3]			± 1
INL [LSB]	[-0.5 1.1]			± 2
Error $\sigma$ [LSB]	2			1
External components	1	4	2 - 3	0

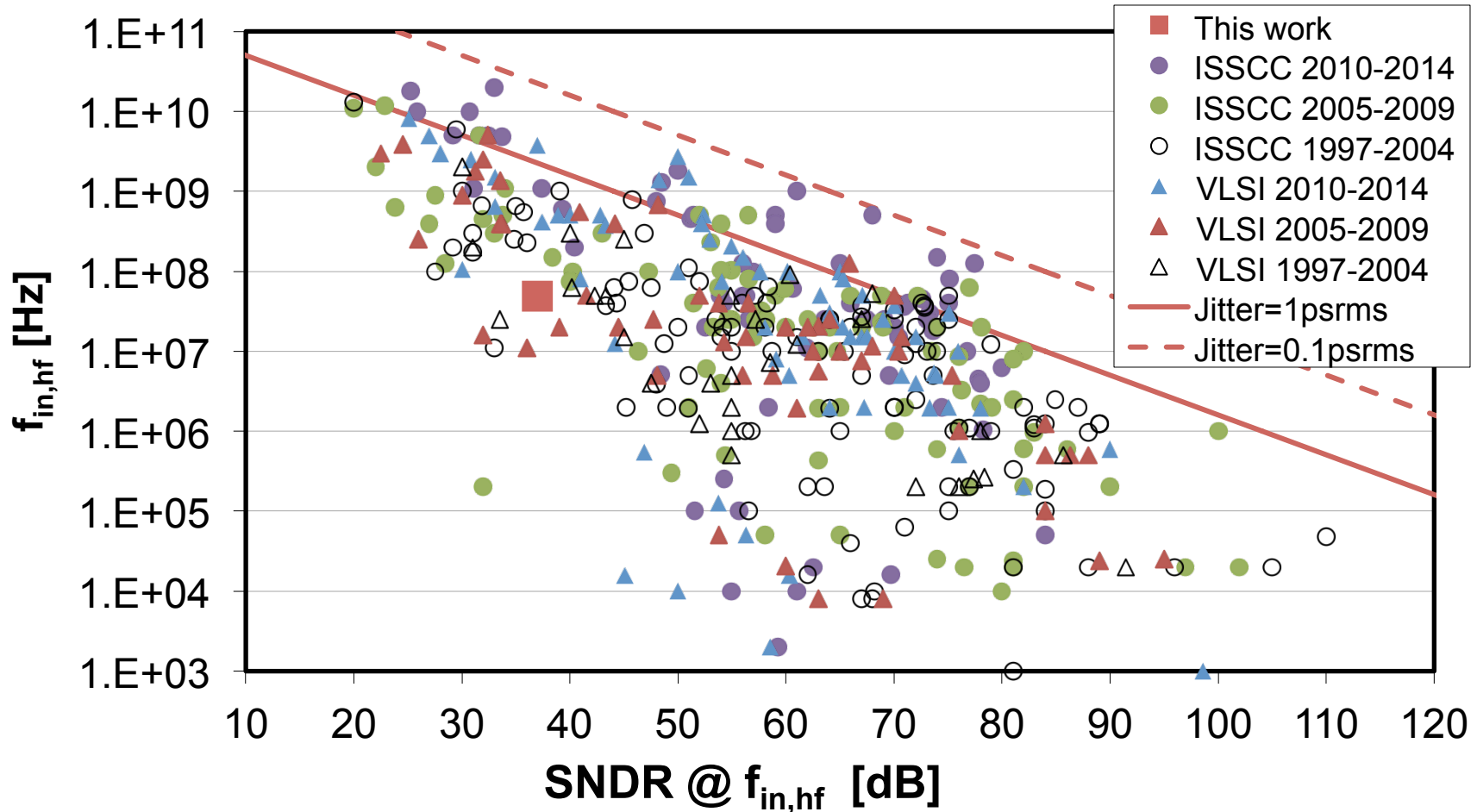
# Comparison with ASIC – Murmann survey

## Conversion energy vs. SNDR



# Comparison with ASIC – Murmann survey

## Signal frequency vs. SNDR



# 4. CONCLUSION

# Conclusion

- Best performing FPGA ADC implemented with 200 MS/s, 6 bits of ENOB and a high linearity.
  - 10×higher sampling rate with 1 bit higher resolution (compared to clock phase TDC based ADC)
  - 200×higher sampling rate with 4 bits lower resolution (compared to Xilinx XADC: found in Xilinx 7 series FPGAs)
  - FPGA ADC can compete with somewhat older ASIC ADCs
- Next steps:
  - 1 GS/s ADC
  - Auto calibration
  - Multichannel
  - DAC



# VHDL Source – Available online

  
**FPGA designs**  
for  
**reconfigurable converters**



Home

FPGA converters

Basic FPGA TDC

Advanced FPGA TDC

FPGA ADC

Contact

## Home



This site offers various designs for reconfigurable FPGA converters. They are all based on Time to Digital Converters. Therefore first an introduction is given into the [basic FPGA TDC](#). It is based on a delay line TDC using the carrychain in the FPGA. For the basic design we will assume a clock synchronous STOP signal and a clock speed > 100 MHz.

This basic FPGA TDC is the basis for both [advanced FPGA TDCs](#) and the proposed [FPGA ADC](#). The advanced FPGA TDC can be used for asynchronous START/STOP signals. The designs are based on a basic TDC with a delay line of 100 ns. The designs are based on a basic TDC with a delay line of 100 ns. The designs are based on a basic TDC with a delay line of 100 ns.

also at 200 MS/s. These were implemented in Xilinx Spartan-3. The designs are based on a basic TDC with a delay line of 100 ns. The designs are based on a basic TDC with a delay line of 100 ns. The designs are based on a basic TDC with a delay line of 100 ns.

minor or major changes, on other Xilinx devices or other FPGA brands. We try to keep an updated overview on papers and other material related to reconfigurable FPGA converters on: [FPGA converters in literature](#). However with the abundance in FPGA TDC papers, the current list only contains a fraction of FPGA TDC publications.

Feel free to [contact](#) us for remarks or questions.

Harald Homulle & Edoardo Charbon

Design by Harald Homulle  
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[http://cas.tudelft.nl/fpga\\_tdc](http://cas.tudelft.nl/fpga_tdc)