Design Space Exploration of L1 Data Caches for FPGA-Based Multiprocessor Systems

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Motivation

Multicore systems are *everywhere*
They have coherent shared memory, caches and operating system support

Objective

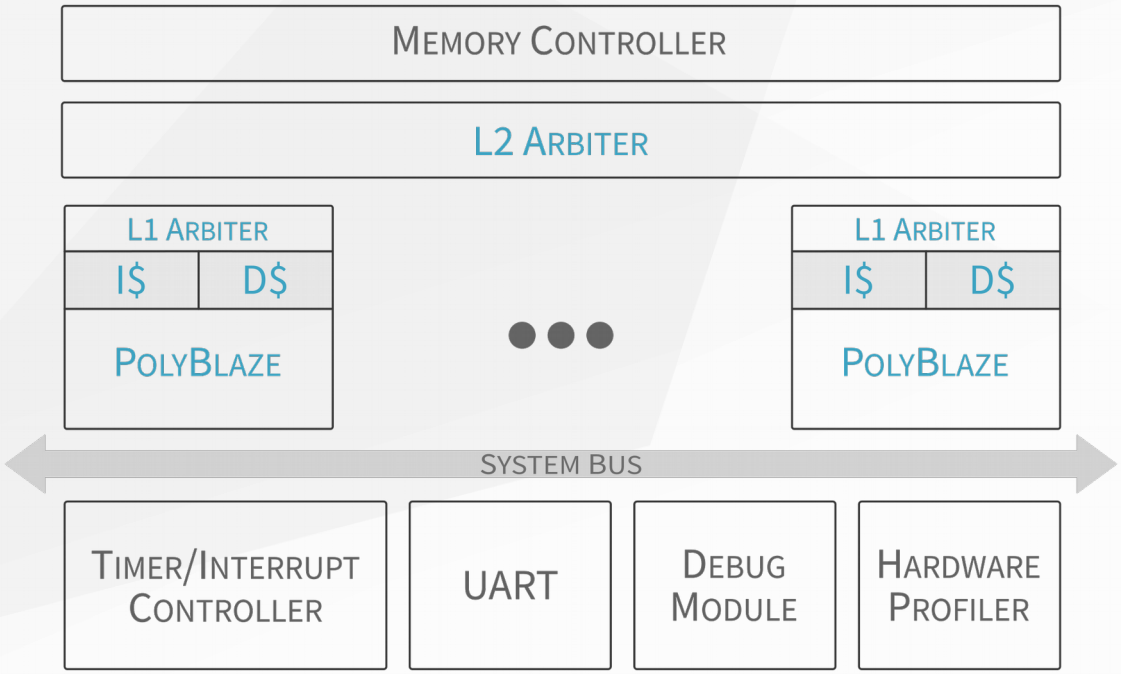
To extend the PolyBlaze framework with a fully coherent, highly configurable L1 cache implementation designed for FPGAs

Performance Efficiency Ratio

$$\text{Perf/Eff Ratio} = \frac{\%\ \text{decrease in runtime}}{\%\ \text{increase in BRAM usage}}$$

Results relative to a **4KB Direct Mapped** cache

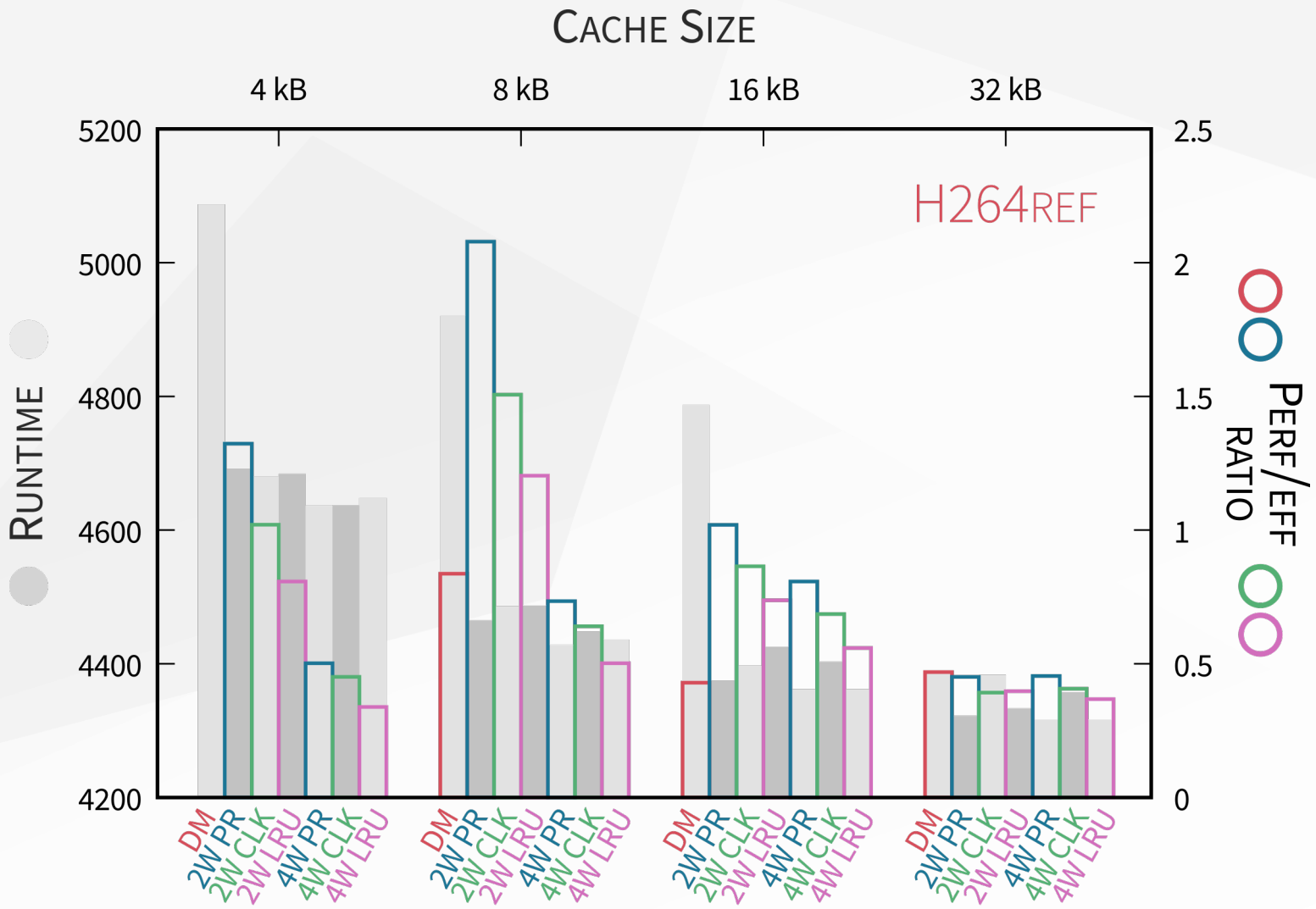
System Design



Cache Properties

- Write Through
- Cache Size **4-32KB**
- Coherency Support
- **1-4** Ways
- Replacement Polices
  - Direct Mapped **(DM)**
  - Pseudo Random **(PR)**
  - Clock **(CLK)**
  - Least Recently Used **(LRU)**

Results & Conclusions



$$\text{Perf/Eff Ratio} = \frac{\%\ \text{decrease in runtime}}{\%\ \text{increase in BRAM usage}}$$

Results relative to a **4KB Direct Mapped** cache

Pseudo Random provides the highest Performance Effeciency Ratio