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# Enhancements in UltraScale CLB Architecture

# FPGA User Requirements

- **Routability** — **Reduce routing demand**
  - Demand for Increased bandwidth requires more routing resources
- **Device Utilization** — **Allow increased utilization of logic resources**
  - Customer want to use as much of the FPGA to maximize device utilization
- **Performance** — **Reduce contribution of routing delays to critical paths**
  - Routing delays dominate critical paths
- **Power** — **Enable power reduction techniques; reduces dynamic power**
  - Large dynamic power

**Changes in FPGA evaluated for positive impact vis-à-vis requirements**

**UltraScale CLB architecture …**

# UltraScale CLB Architecture Enhancements

- **Several enhancements in UltraScale vis-à-vis 7-Series Architecture**
  - Enhancements in BRAM, DSP and other logic blocks
  - More flexible Clocking
  - Improvements in Routing Architecture
  - Improved inter-die connectivity
  - Larger Carry Chain in CLB
  - Larger Multiplexer in CLB

- **We only discuss**
  - Better access to flops
  - Better use of flops

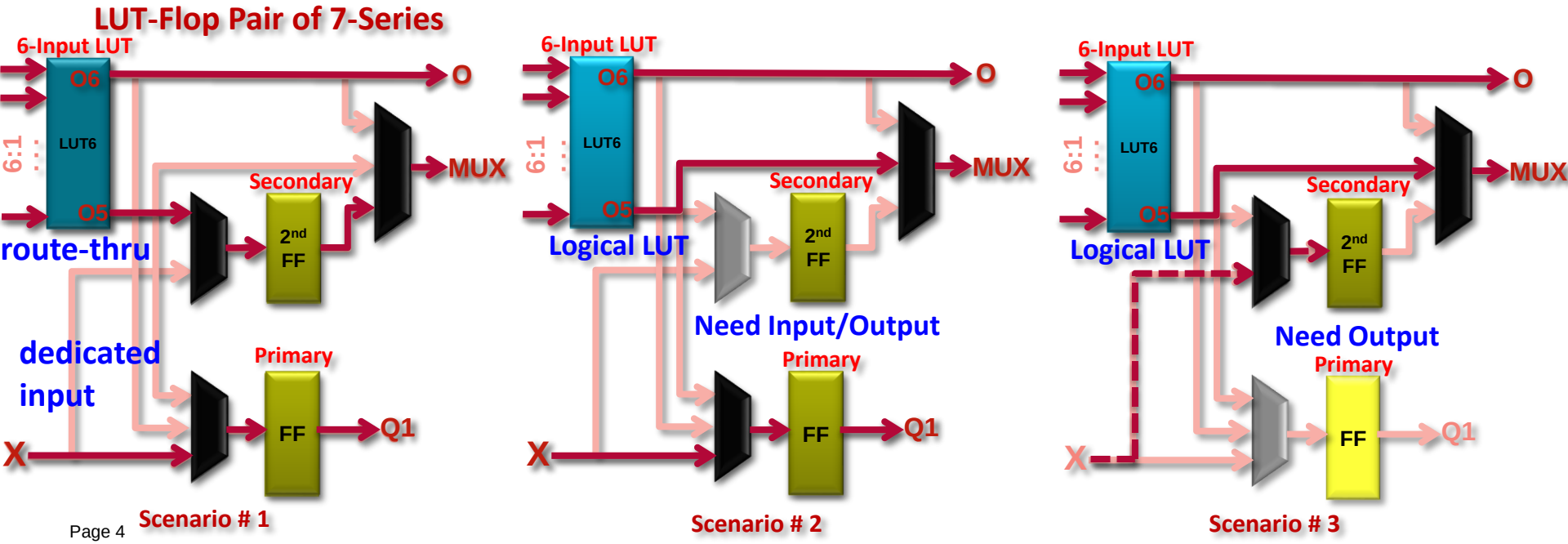
**CLB changes should result in:**
- **Lower demand for routing resources**
- **Fewer CLBs**
- **Less impact on the QOR due to increased device utilization**

# Opportunities for improvement in 7-Series CLB

## Make flops more *accessible*

- In 7-Series CLB Architecture:
  - "LUT route-thru" needed to access both flops simultaneously
  - Extra input/output needed to escape all LUT and Flop outputs simultaneously

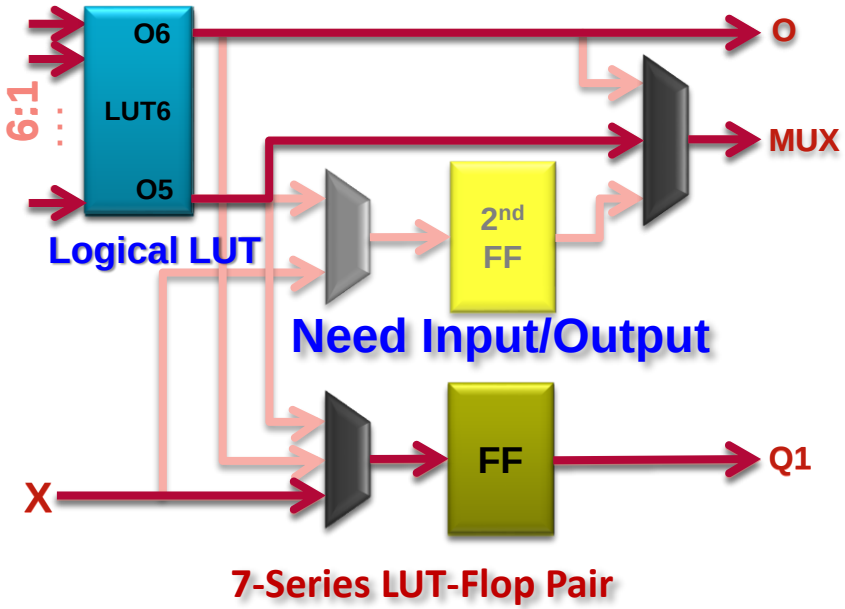
## Opportunity to improve packing in 7-Series CLB

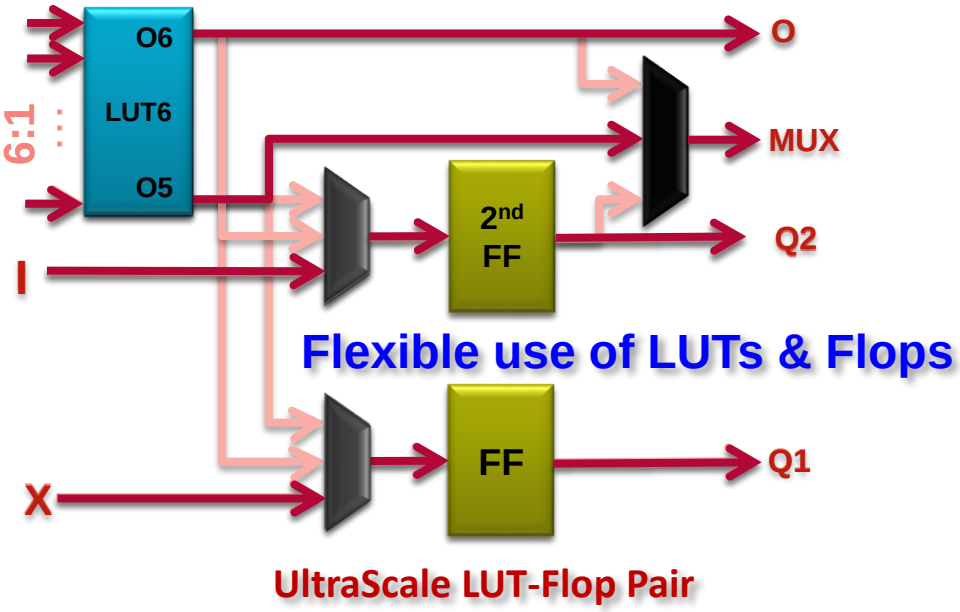


# Flops More Accessible in UltraScale CLB

- Flop and LUT counts unchanged in UltraScale CLB
- Additional input to 2nd FF removes dependence on LUT route-thru
- Additional output enables 2nd FF independent access to routing

## LUTs and 2 Flops usable simultaneously

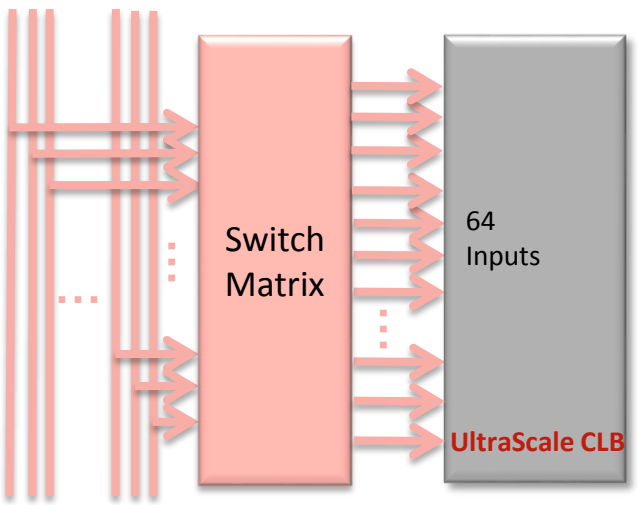


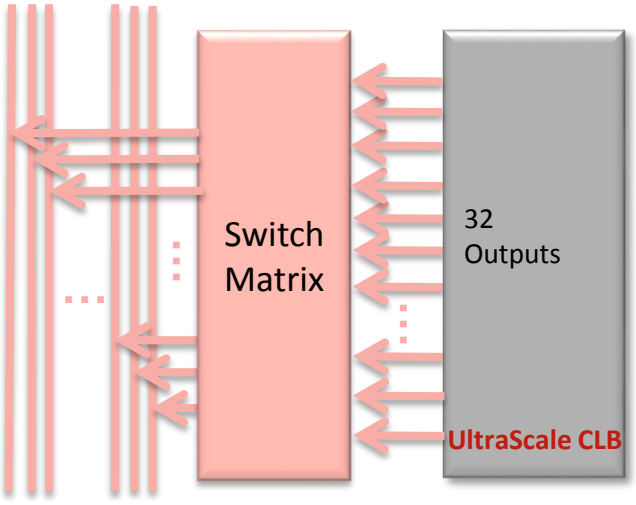
# Effect of Increased Accessibility to Flops

- **Independent access to/from flops**
  - Input ports increased from 60 to 64
  - Output ports increased from 24 to 32
- ***No additional input muxes***

**More CLB flexibility → Borrowed connectivity from Input/Output**




**Re-use of existing multiplexers to serve new inputs**



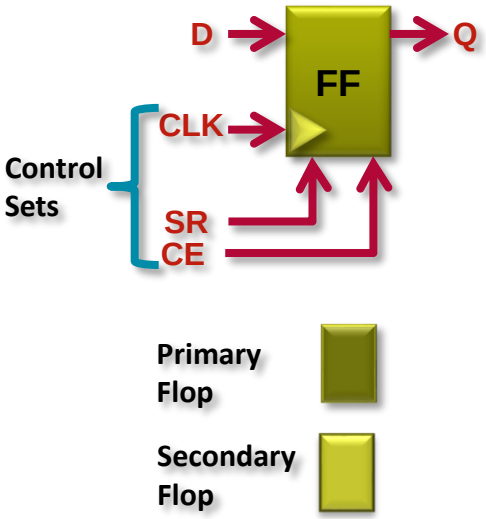

**Proportional reduction in capability of existing outputs**

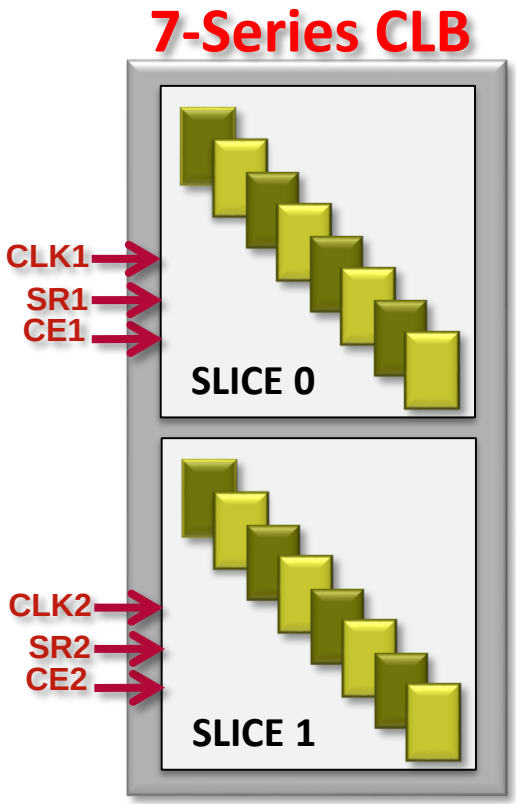
# Opportunity for improvement in 7-Series CLB

## Make flops more *usable*

- Combination of signals driving Clock, Set/Reset, and CE of a flop
- 7-Series CLB offers 2 Control Sets per CLB

## Control sets limit packing of flops in a CLB

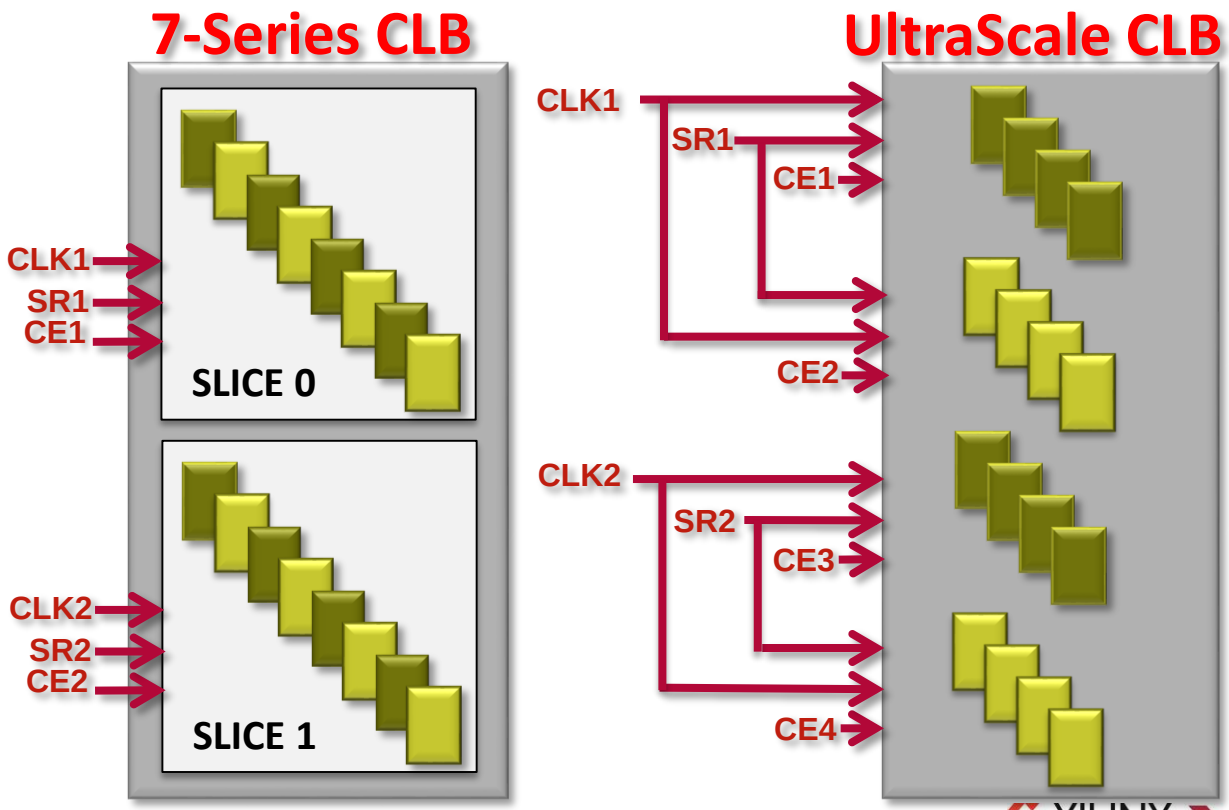


# Flops More Usable in UltraScale CLB

- 2 Extra CEs and 4 Control sets per CLB in UltraScale
- Design's packing is mostly limited by its clock enables

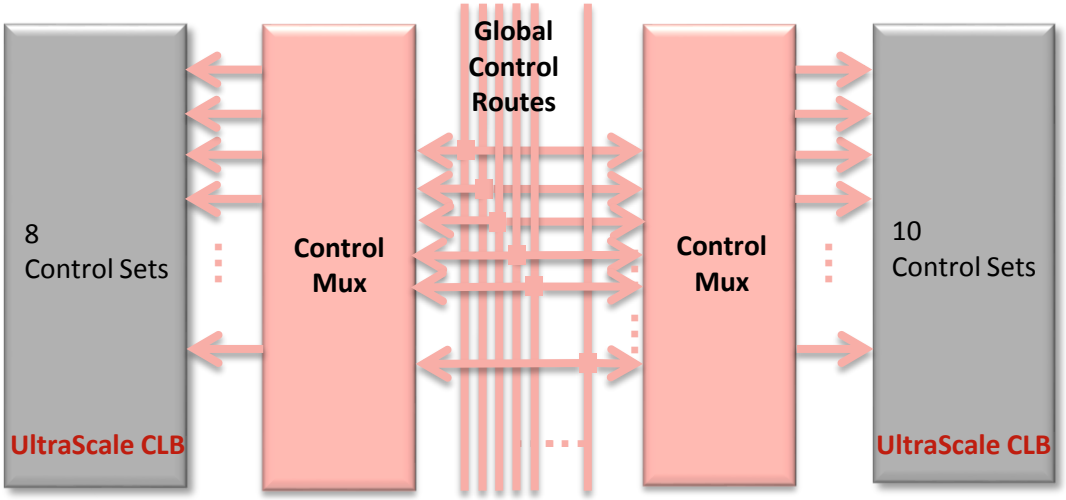
## More flops can be packed into UltraScale CLB



# Effect of Increased Usability of Flops

- Global control routes increased from 12 to 16
- Control muxes increased by 5

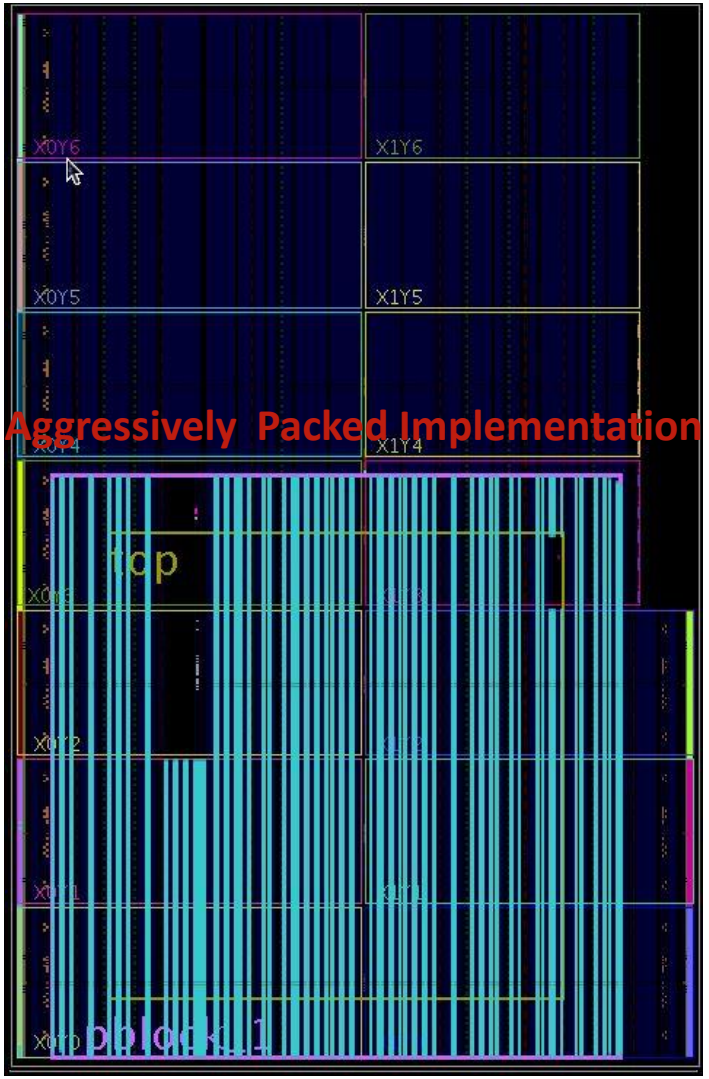
## Added usability with additional Control Routing and Muxes



# Experimental Setup

# Experimental Setup

- **Used Customer designs and IPs**
  - 10K to 200K Flops
  - 30 K to 160K LUTs
  - Also BRAM, DSP, Control Sets
  - Wired, Wireless, Video and Audio processing
- **Customers like to "use all CLBs they pay for"**
- **Used aggressively packed implementation**
  - Forces placer to use additional CLB flexibility
  - Demonstrates benefit of CLB enhancements
- **Used progressively smaller area constraints**
  - Discover tightest packing possible




Aggressively Packed Implementation

99% LUT Utilization

## Premise

- **UltraScale should handle tighter packing more gracefully**

# Experiment Setup

## Isolating effect  of CLB enhancements only

### Modifications to design implementation flow

- Designs only placed, to avoid effects of different routing architectures
- Placer does not respond to the routing architecture
- Placer uses identical delay models
- Estimated post-place FMAX

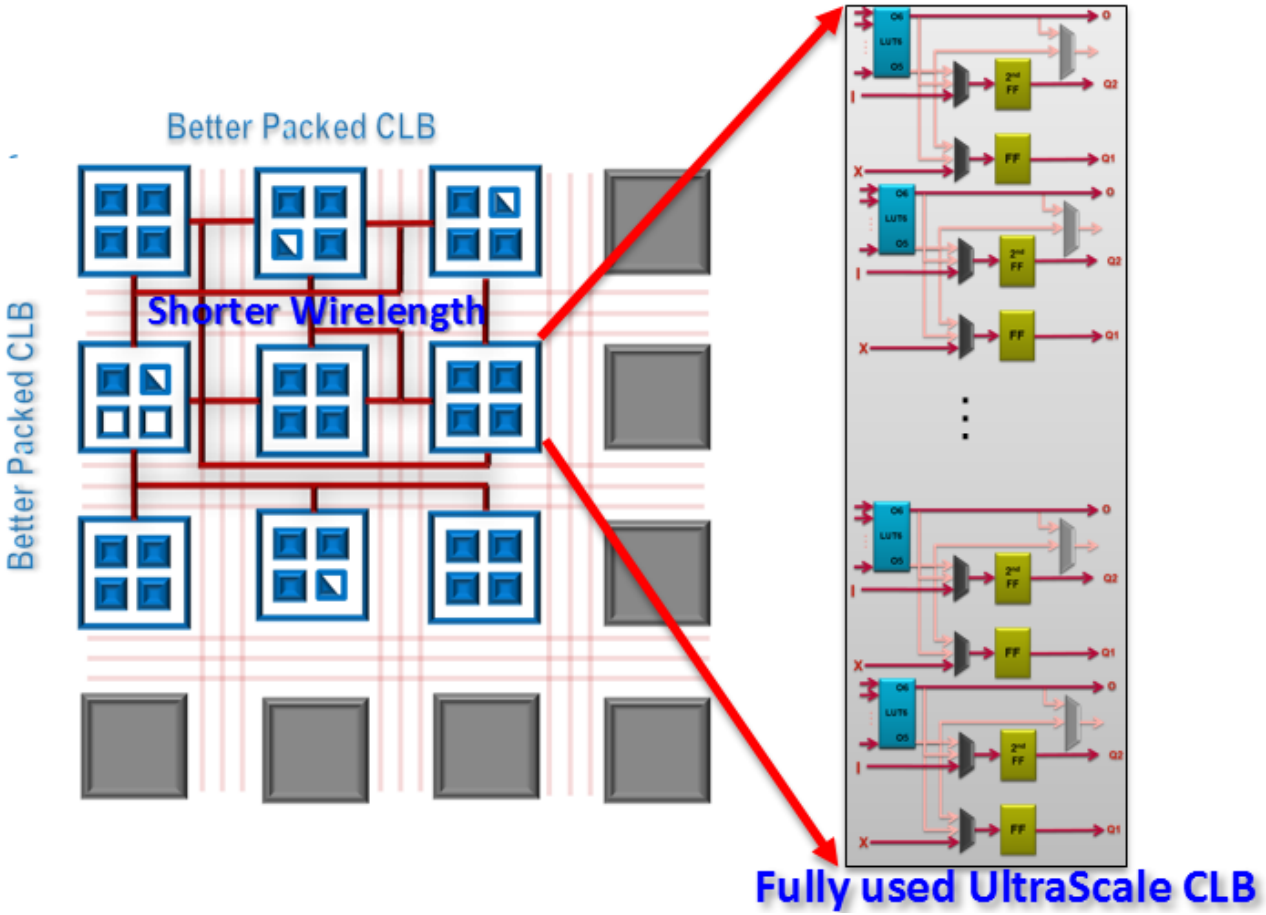
***Show effect of only CLB Changes***

# Results

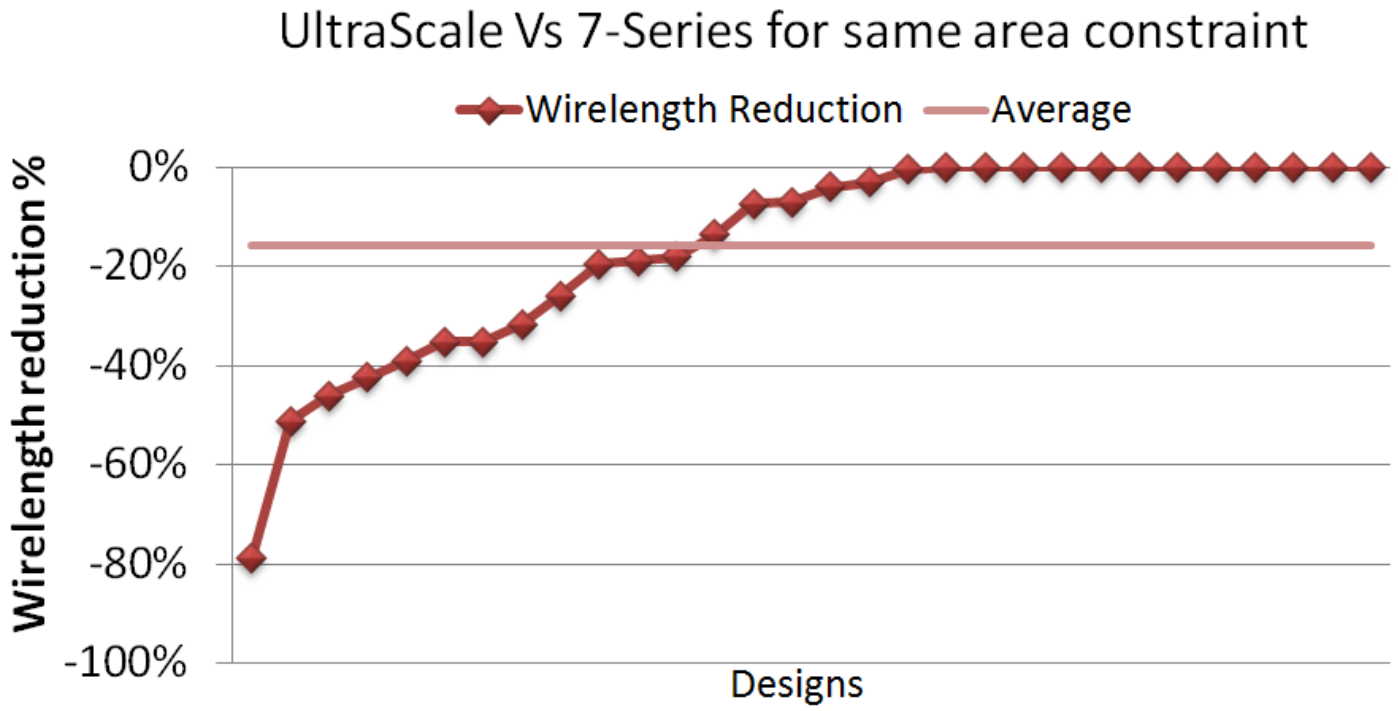
Benefits on Routability, Device Utilization, Performance & Power

# Routability

- Measure *demand for routing*
  - Predicted through wirelength of the placement
  - Wirelength measured in Manhattan bounding box
- Shorter wirelength with better packing

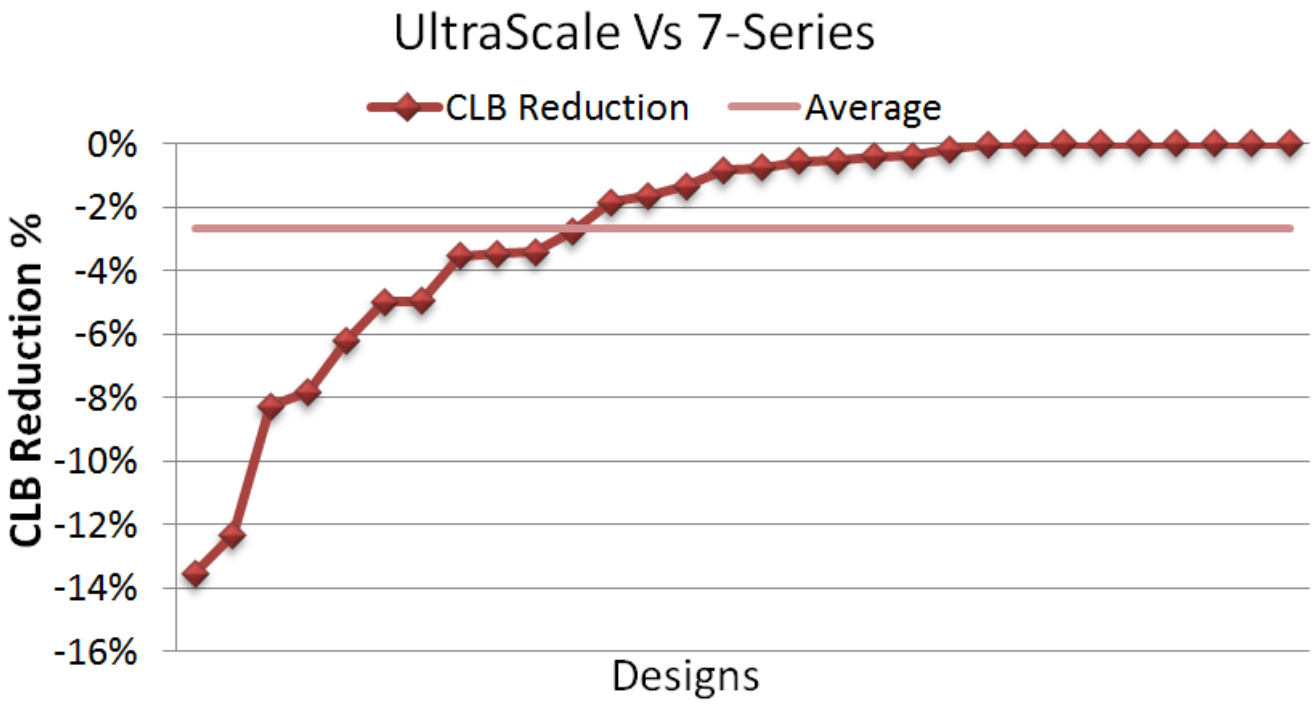


# Routability




- Avg. 16% shorter wirelength than 7-Series
- Reduced routing demand:
  - Reduced routing power dissipation
  - Better performance
  - Also benefit complex and wider bus design
- Addresses routability by reducing the demand for routing

# Device Utilization



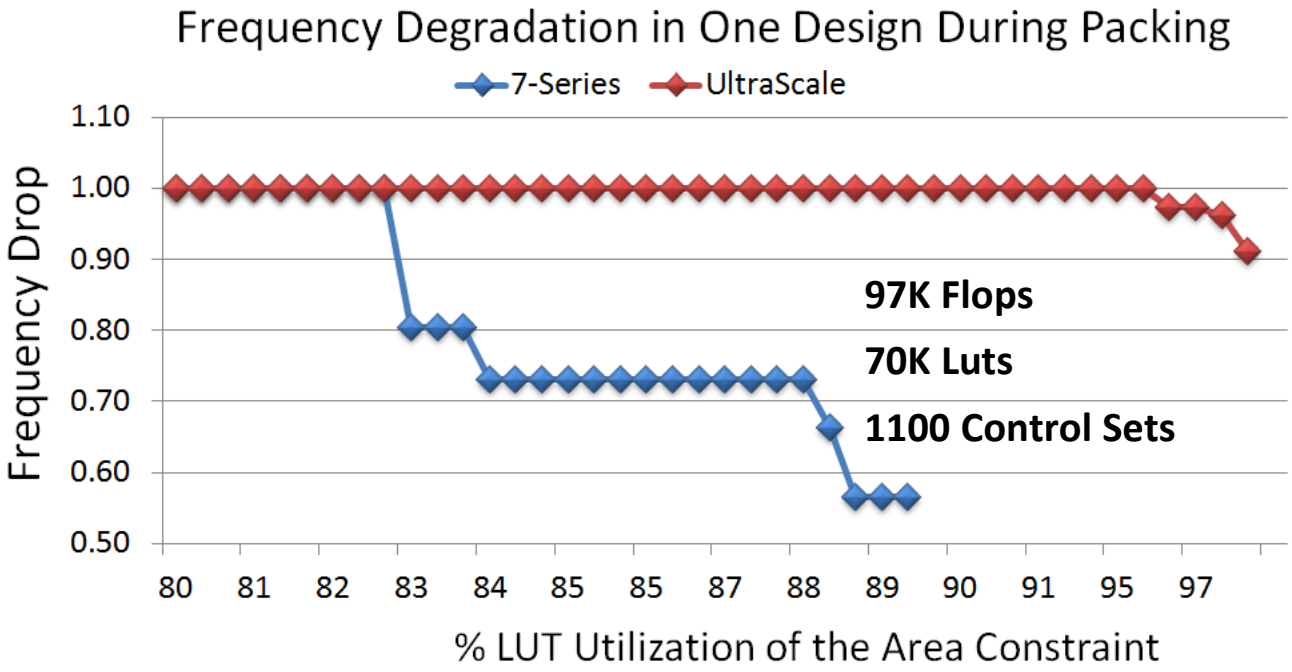

- **Average: 3% fewer CLBs**
- **Best case: 14% fewer CLBs**
- **Visible savings in more restricted designs**
- **Less savings when:**
  - Fewer flops with independent access
  - Fewer control sets
  - Fewer LUT merging
  - Or, CLB utilization dominated by Carry and Multiplexers

# Device Utilization with Pipelining

## Pipelining data paths will:

- Improve performance
- More flops with independent access
- Even more saving with enhanced access to 2nd FF

# Performance

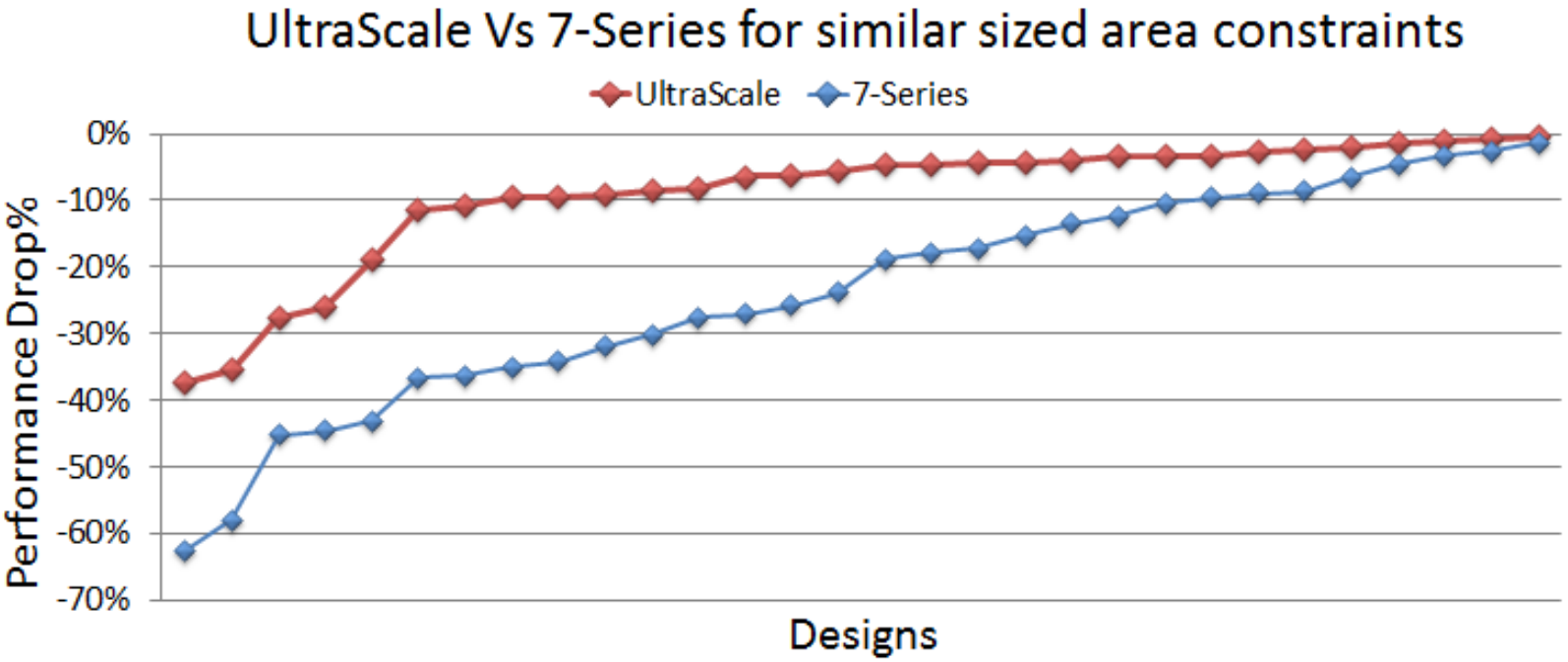



- Performance vs legal placement trade off
- Performance tradeoff determines CLB flexibility

**7-Series CLB offers high device utilization, UltraScale offers even higher with less performance degradation**

- 7-Series
  - Supports up to 80% LUT utilization
  - Maintain performance within 20%
  - Significant improvement over 40nm family
- UltraScale
  - Close to maximum LUT utilization
  - Maintain performance within 12%

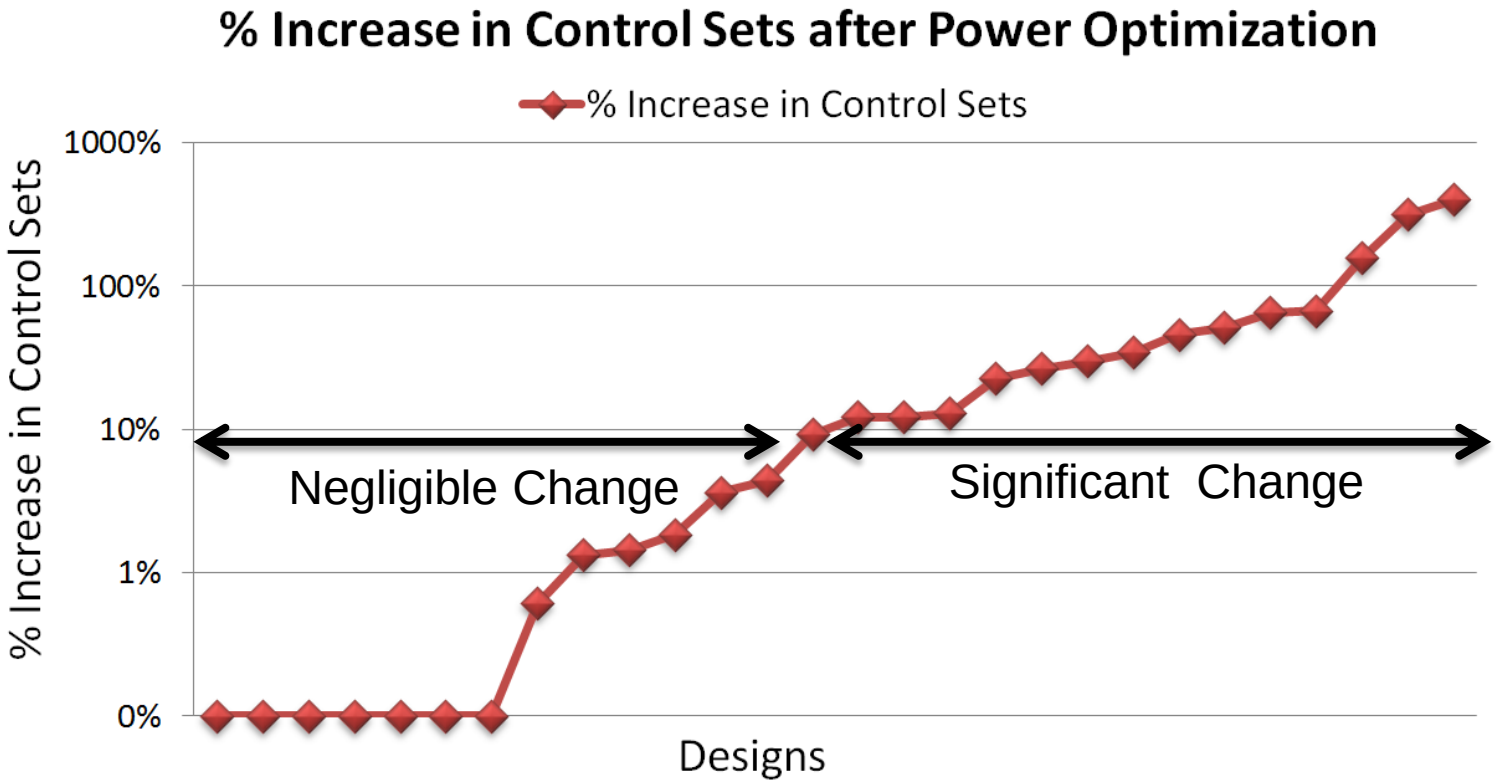
# Performance




- Average 9% vs 24% performance degradation
- Post placement frequency estimates
- Routing will show routing architecture effects
- Performance trend to sustain even after routing

**UltraScale CLB minimized performance degradation due to tight packing**

# Effects of Power Optimization




- Synthesizes extra clock enable, If a flop output is not used every clock cycle
- Depends on design's characteristics
- No adverse impact of extra control sets on the CLB Reduction

# Conclusion

- **Addressing the challenges of future design:**
  - Achieve higher bandwidth and maintain routability
  - Achieve higher device utilization
  - Achieve performance target
  - Achieve requisite power budget
- **UltraScale CLB has same number of LUTs and Flops**
  - It can now use them effectively
- **Addresses the demand of routing resources with a flexible CLB**
- **UltraScale CLB is more flexible to handle these challenges**

# Thank You!

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