RapidSmith 2: A Framework for BEL-level CAD Exploration on Xilinx FPGAs

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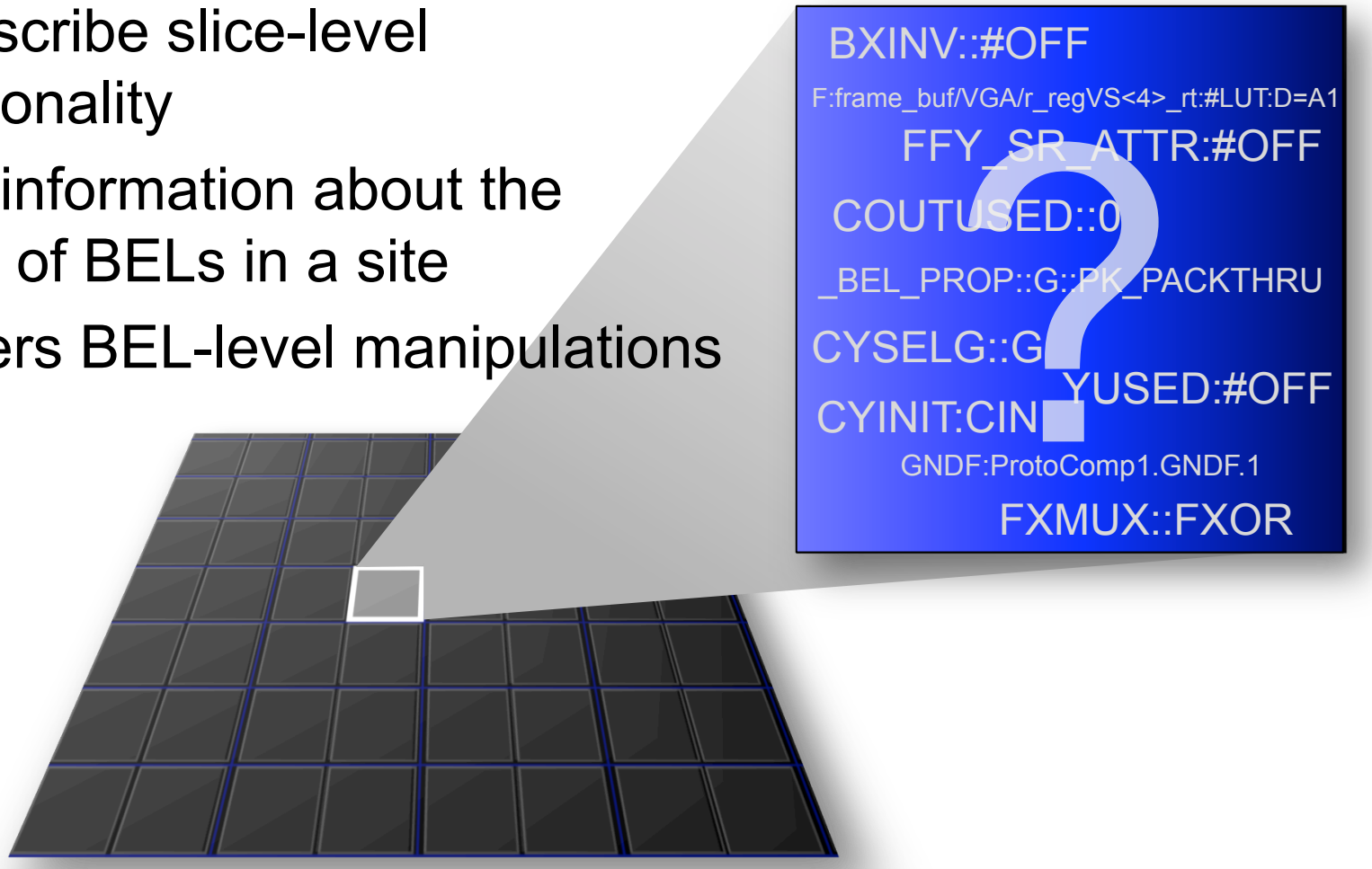
RapidSmith 1

- Framework for modifying Xilinx XDL designs
- Contain components and routing of Xilinx chips
- Supports large number of research topics including
  - Rapid design prototyping flows
  - Reliability and fault-tolerant techniques
  - PR frameworks
  - Post-PAR debug
  - FPGA security

RapidSmith 1 Limitations

- RapidSmith uses string attributes to describe slice-level functionality
- Little information about the types of BELs in a site
- Hinders BEL-level manipulations



RapidSmith 2 Improvements

- Adds BEL types, properties, and interconnectivity
- New BEL-level netlist
- Tools to convert between XDL and BEL-level netlist
- Allows modifying the packing of a design
- Provides functionality for packing, placing, and routing a synthesized netlist onto Xilinx FPGAs