Area and Delay Trade-offs in the Circuit and Architecture Design of FPGAs

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FPGA Cost and Performance Trade-offs

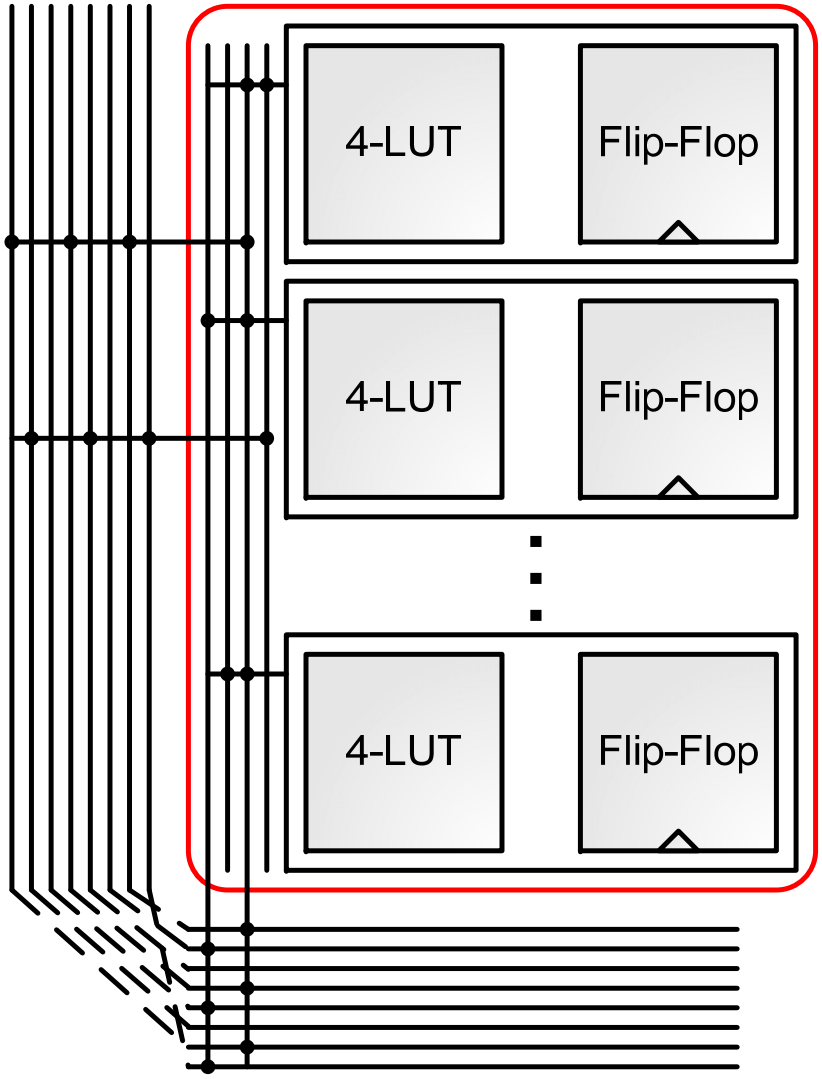
- FPGAs cater to a wide range of markets
  - Different area/cost vs. performance requirements
  - Not served by a single family

- FPGA vendors now offer 2 or more families
  - Altera: Stratix → Cyclone
  - Xilinx: Virtex → Spartan
  - Lattice: LatticeSC → LatticeECP2/M

Trade-offs Using Logical Architecture

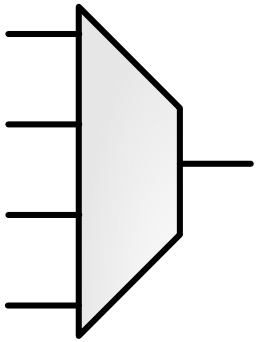
- Cluster size
- LUT Size
- Special-purpose blocks

- Well studied

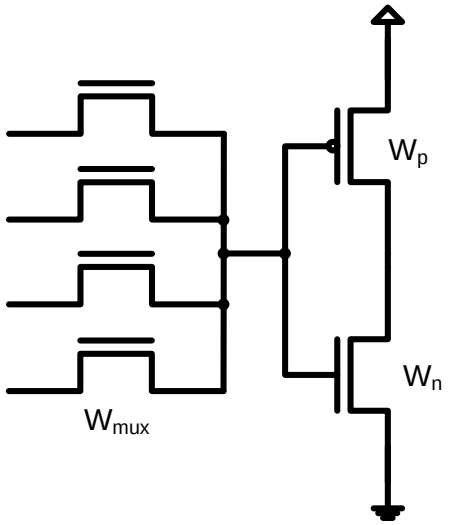


Trade-offs Using Electrical Design

- Circuit structure
- Transistor Sizing



- Not as well studied for FPGAs



Goals of This Work

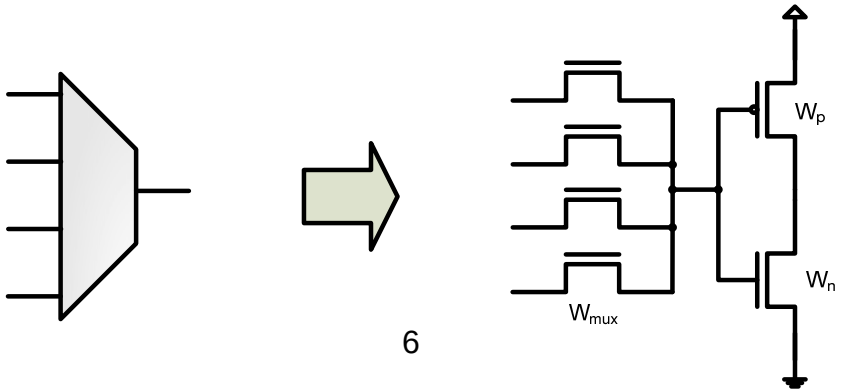
- Explore Area-Delay Trade-offs of all three:
  - Logical Architecture
  - Circuit Topologies
  - Transistor Sizing

- Want parameters with greatest leverage

Exploring Trade-offs

- Logical Architecture → VPR
  - New version with modern single driver routing

- Electrical Design → ?
  - Past manual approaches not feasible for considering hundreds of architectures
  - Need automated tool to facilitate exploration



Electrical Design of FPGAs

- No automated design tools for FPGAs exist
- ASIC/Custom tools not appropriate

- Unique challenges with FPGAs
  - Programmability
    - Don’t know **what** end-user design will be implemented
  - Repeated Components
    - Just a few unique cells are repeatedly interconnected

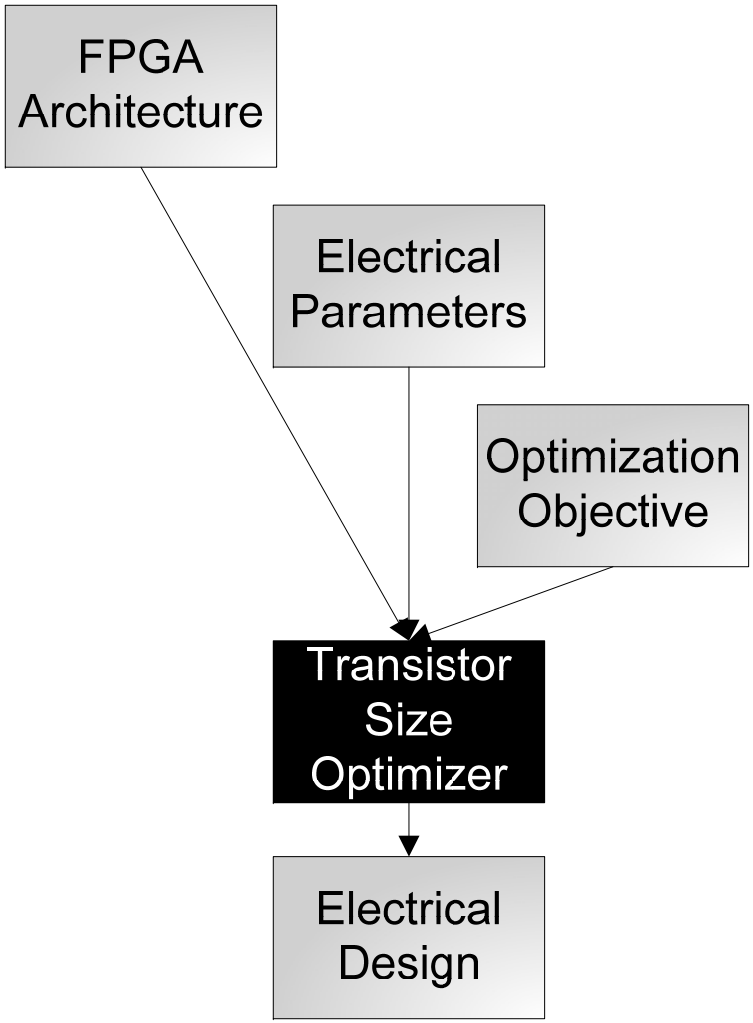
- Developed automated sizing tool for FPGAs

Automated Transistor Sizing for FPGAs

- Cluster Size
- LUT Size
- Routing Topology

- Process Technology
- Mux Structure

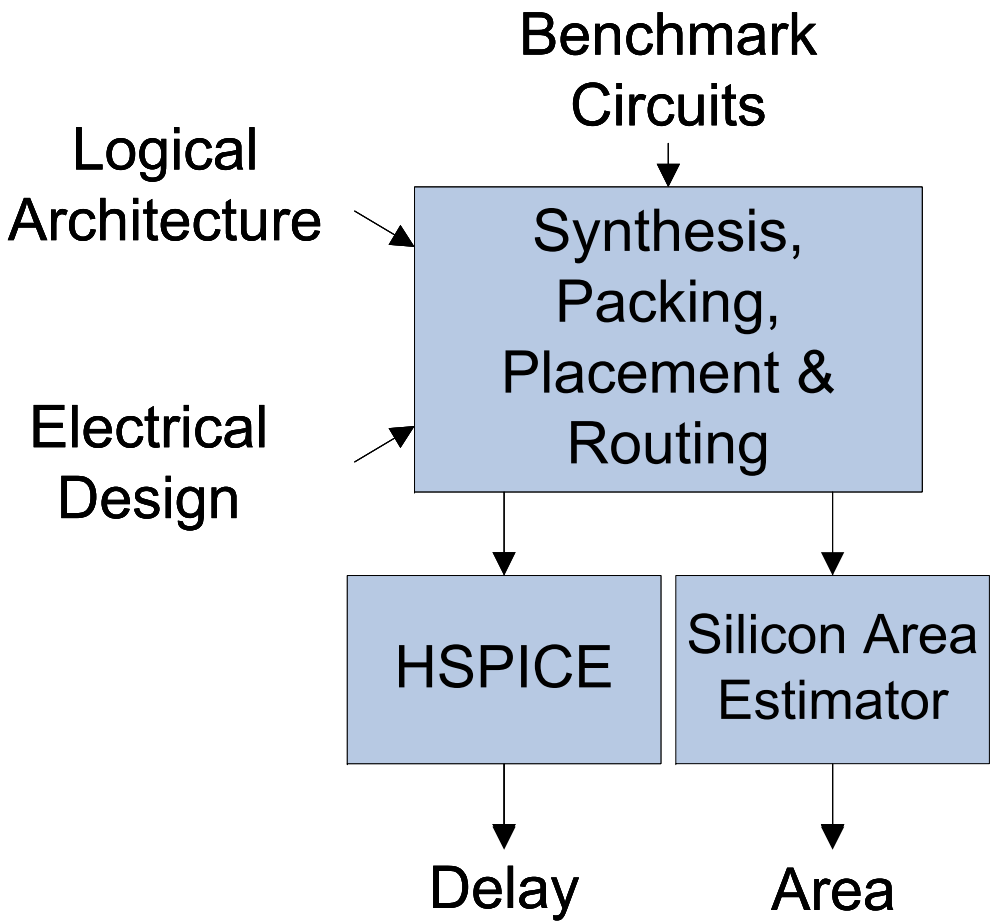
- Area
- Delay
- AreaDelay



Measuring Area and Delay after Design Changes

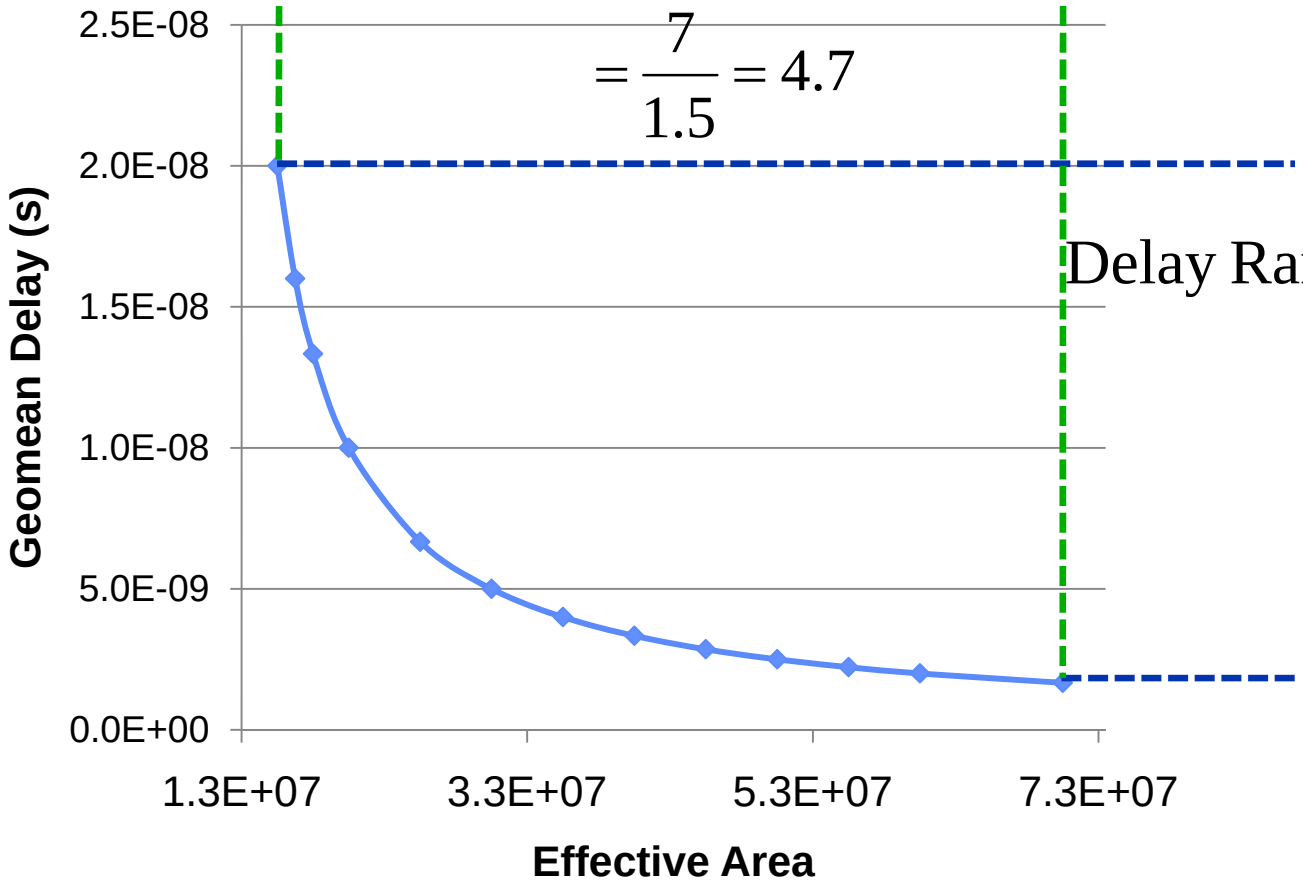
- Transistor sizing gives area/performance of FPGA's **components**
- Need full experimental flow to gauge **effective** area/performance

Area and Delay Measurements



Measuring Trade-off Sizes – Example

$$\text{Area Range} = \frac{\text{Largest Design}}{\text{Smallest Design}}$$



$$\text{Delay Range} = \frac{\text{Slowest Design}}{\text{Fastest Design}}$$

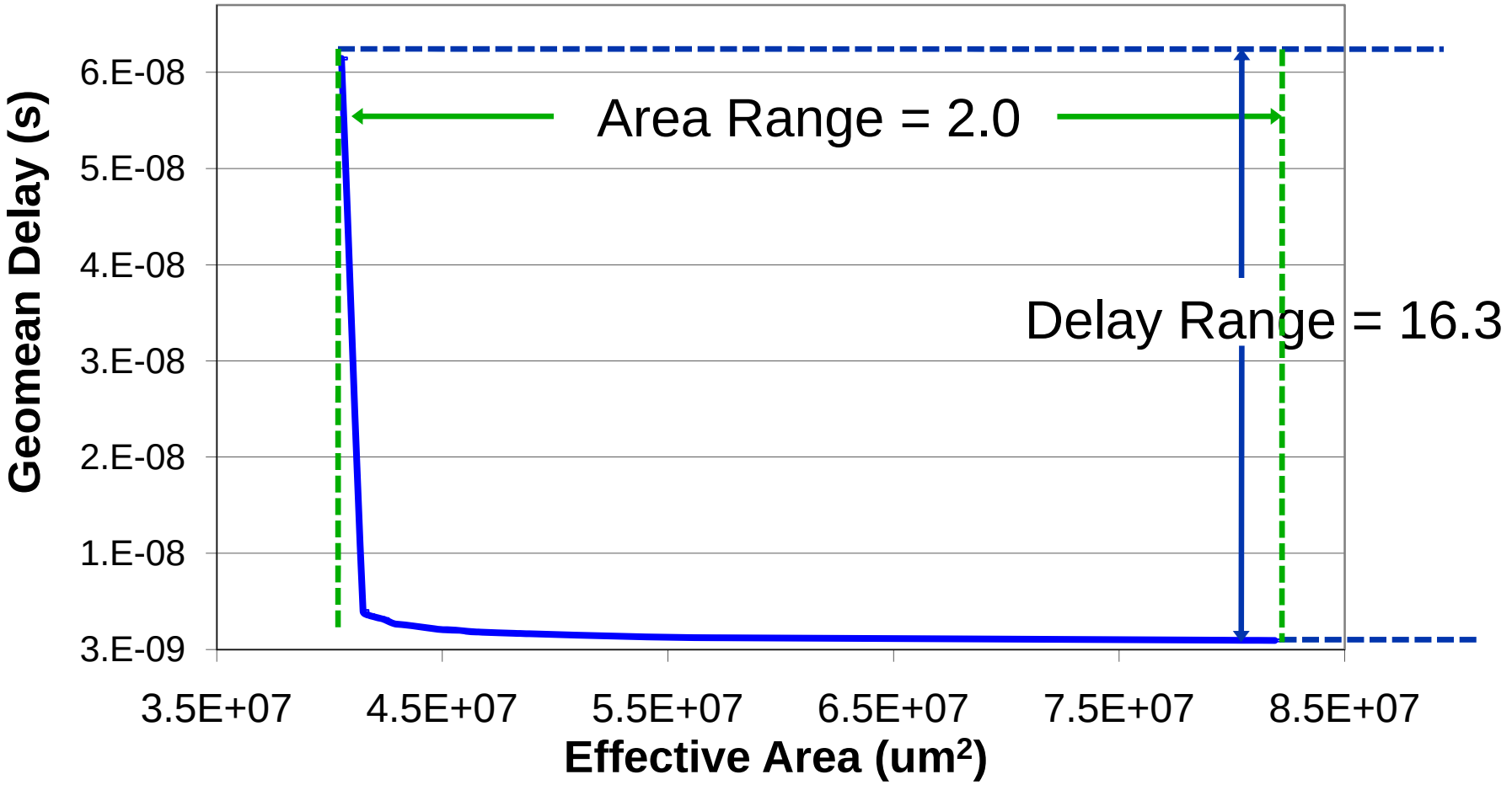
$$= \frac{20.0}{1.7} = 12$$

Results

- Geomean delay across 20 MCNC circuits
- 90 nm CMOS

Area-Delay Trade-offs with Transistor Sizing

- Transistor sizing for single architecture



Range of Area Delay Trade-offs

	Delay Range	Area Range
Transistor Sizing	16.3	2.0
Cluster Size (1-10) [Ahmed04]	1.6	1.5
LUT Size (2-7) [Ahmed04]	2.2	1.5
Segment Length [Betz99]	1.6	1.6
Cluster and LUT Size [Ahmed04]	3.2	1.7

- Transistor sizing offers more range but area and delay are imbalanced

What Trade-offs are Interesting?

- Too slow or too large → design is unrealistic
  - Unreasonable to sacrifice 10X performance for a small area reduction

- Restrict focus to more balanced trade-offs

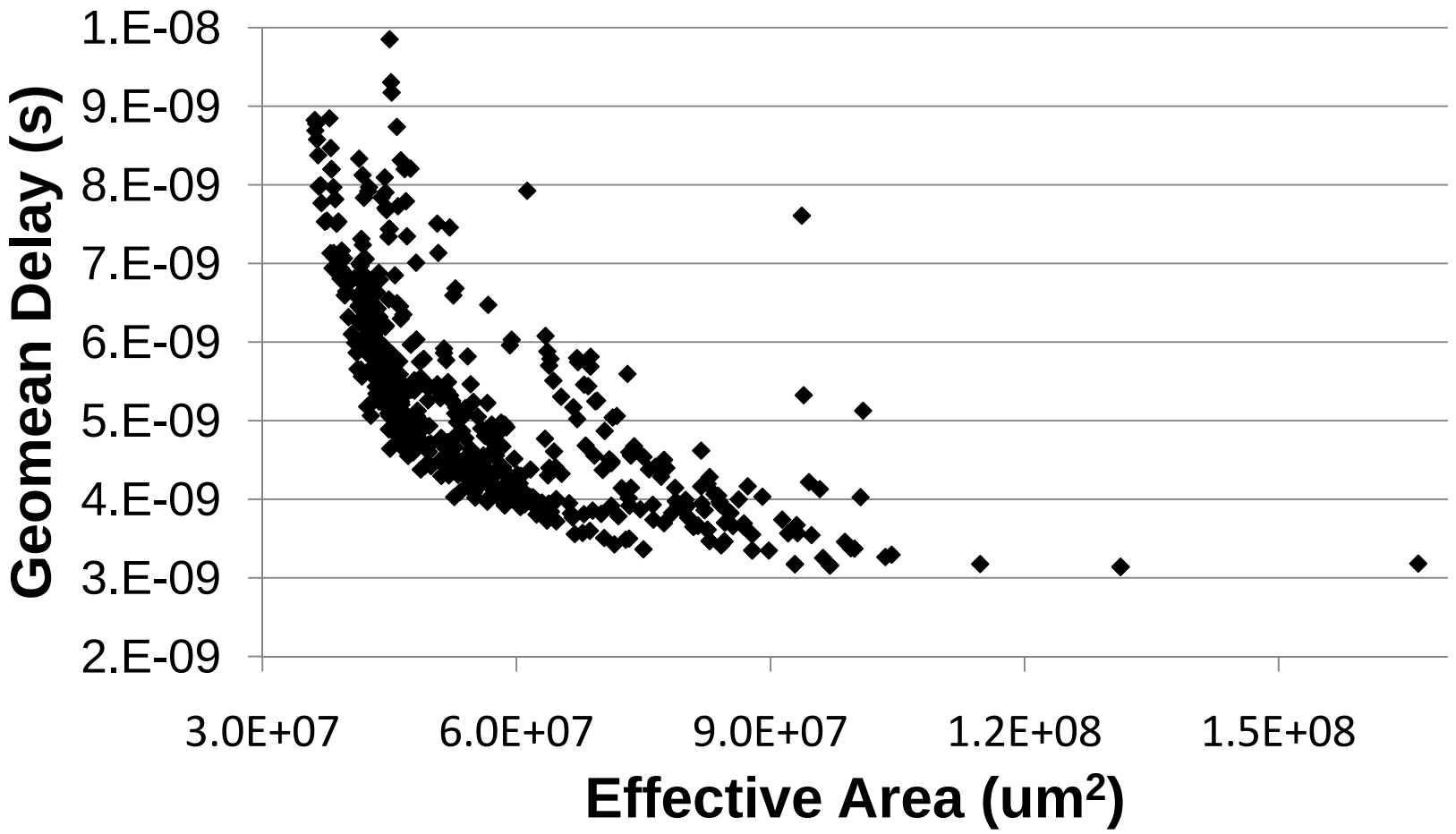
$$-3 < \frac{\%\ Delay\ Change}{\%\ Area\ Change} < -\frac{1}{3}$$

Interesting Trade-offs

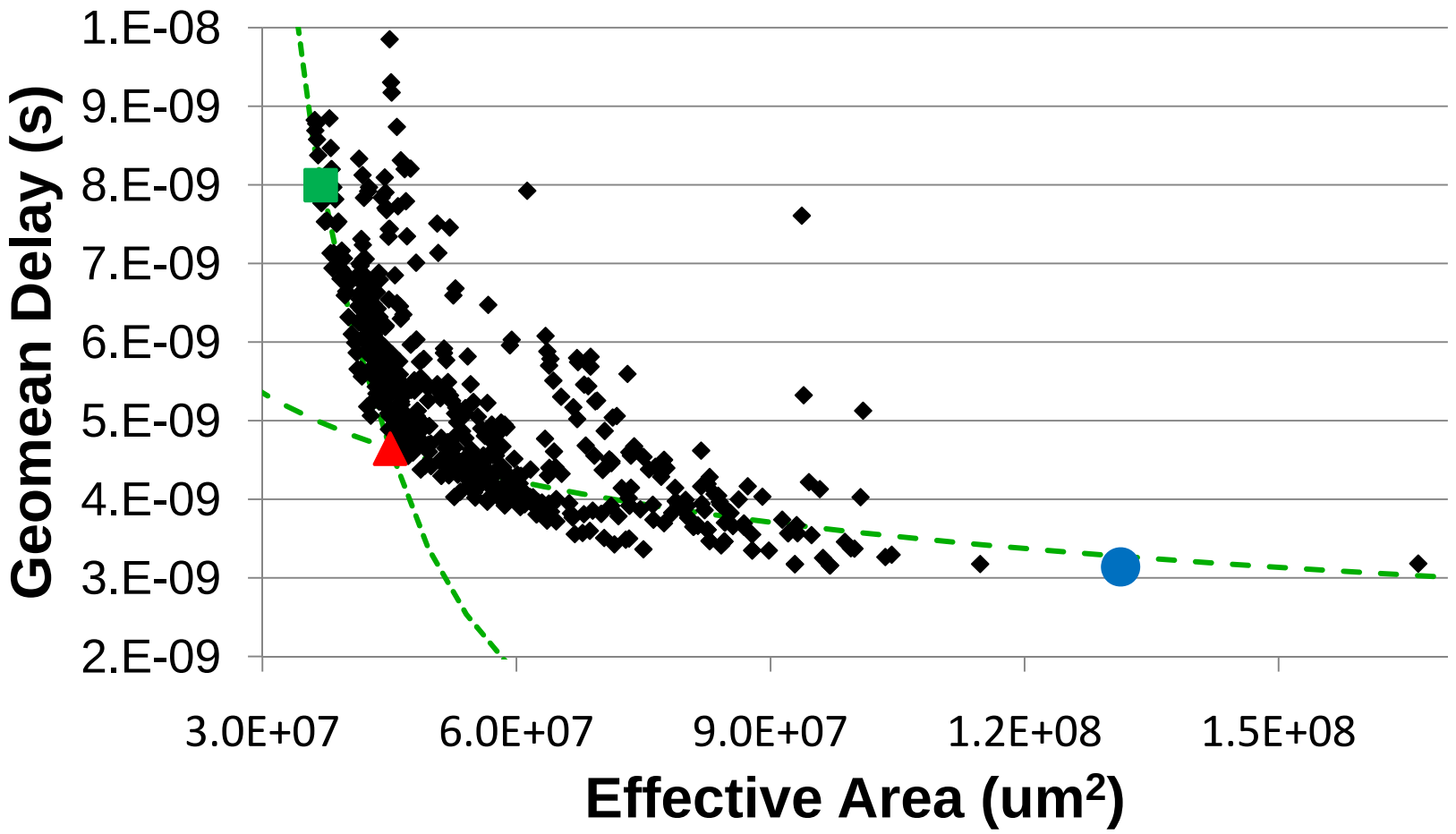
	Delay Range	Area Range
Transistor Sizing	1.3	1.2
Cluster and LUT Size [Ahmed04]	1.2	1.1

- Transistor sizing provides significant leverage
- But we can also vary architecture!

Trade-offs with Architecture & Transistor Sizing



Trade-offs with Architecture & Transistor Sizing



Transistor and Architecture Trade-offs

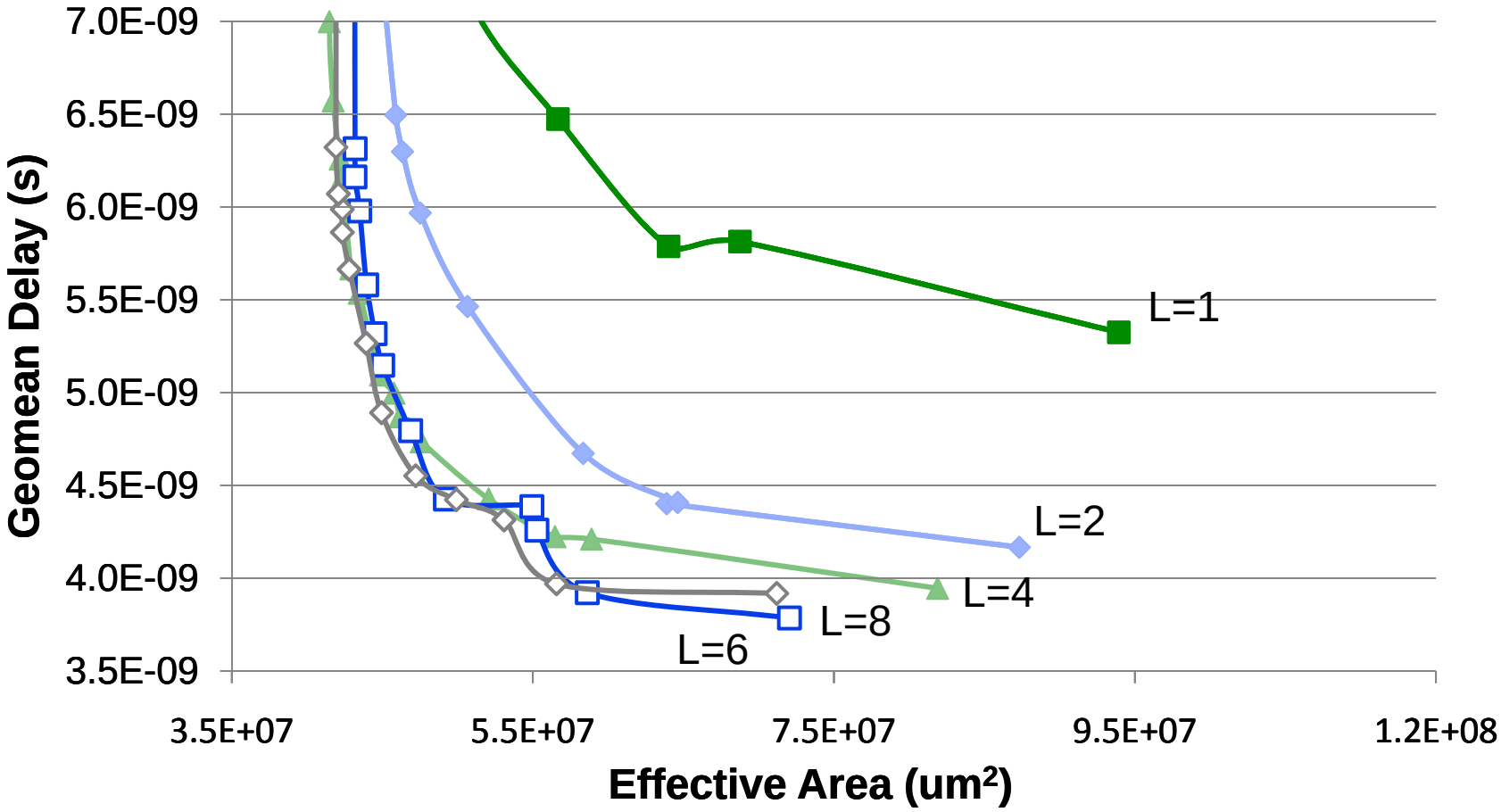
	Delay Range	Area Range
Transistor Sizing & Architecture	3.6	2.6
Cluster and LUT Size [Ahmed04]	1.2	1.1

- Design space is large

Architecture and Area-Delay Trade-offs

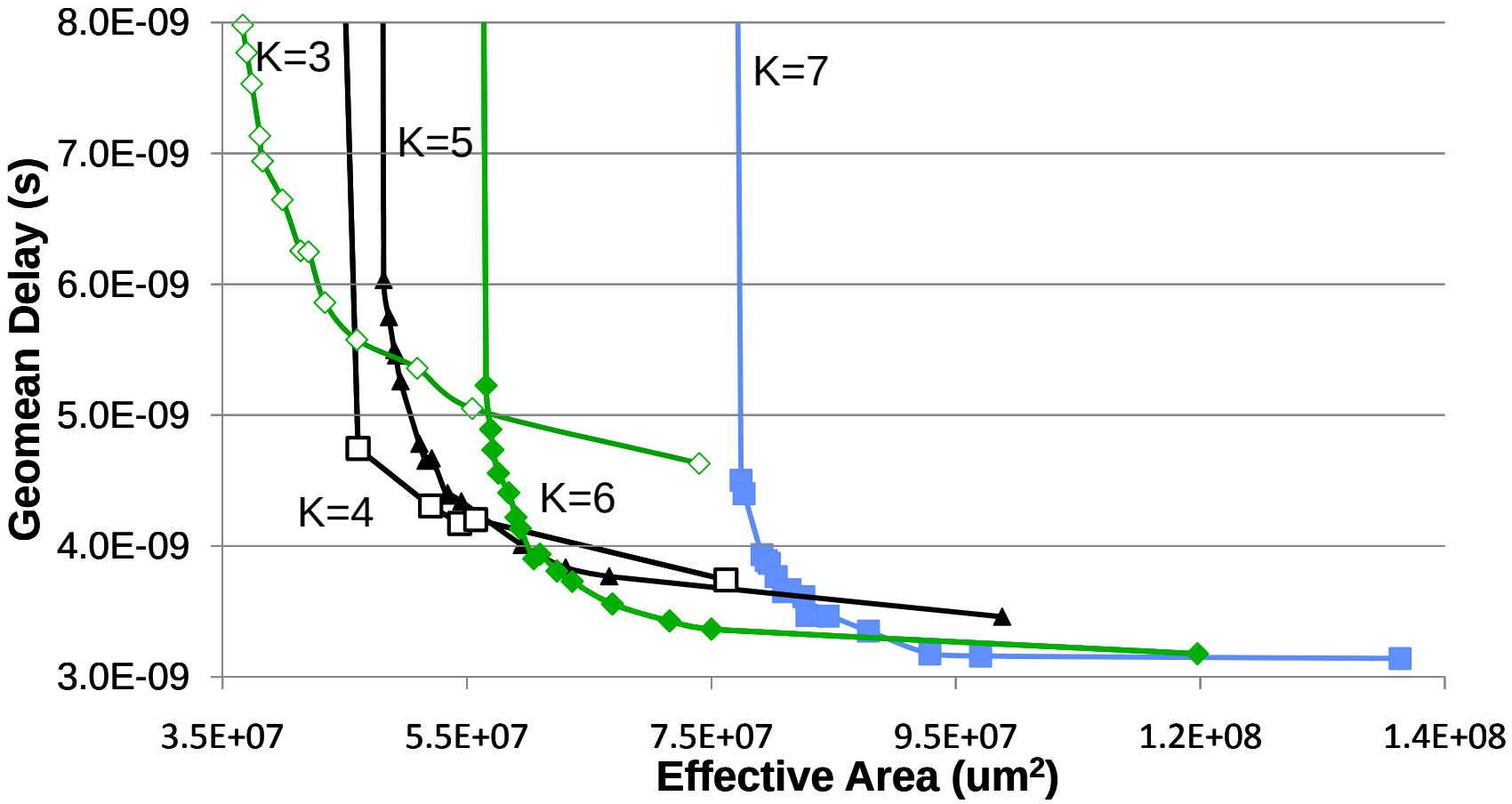
- LUT Size
- Cluster Size
- Segment Length

Trade-offs with Segment Length



- Limited trade-offs possible with segment length

Trade-offs with LUT Size



- Varying LUT Size enables useful trade-offs

Conclusions

- Design space is large
  - Even when restricted to useful trade-offs!
- Transistor sizing is an important lever for trading-off area and delay
- LUT Size is best parameter for trade-offs at architecture level

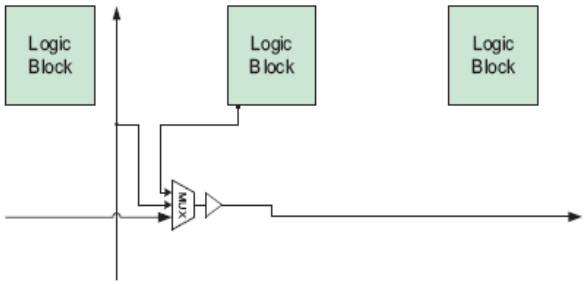
VPR

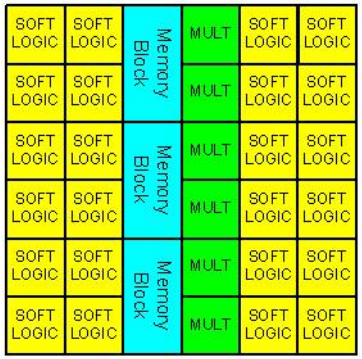
- VPR is the placement and routing tool underlying this work and many others
  - But VPR v4.3 does not support now standard architectural features

- New Version, VPR 5.0, now in Beta
  - Supports more architectural features
  - Maintains quality and architectural exploration capabilities

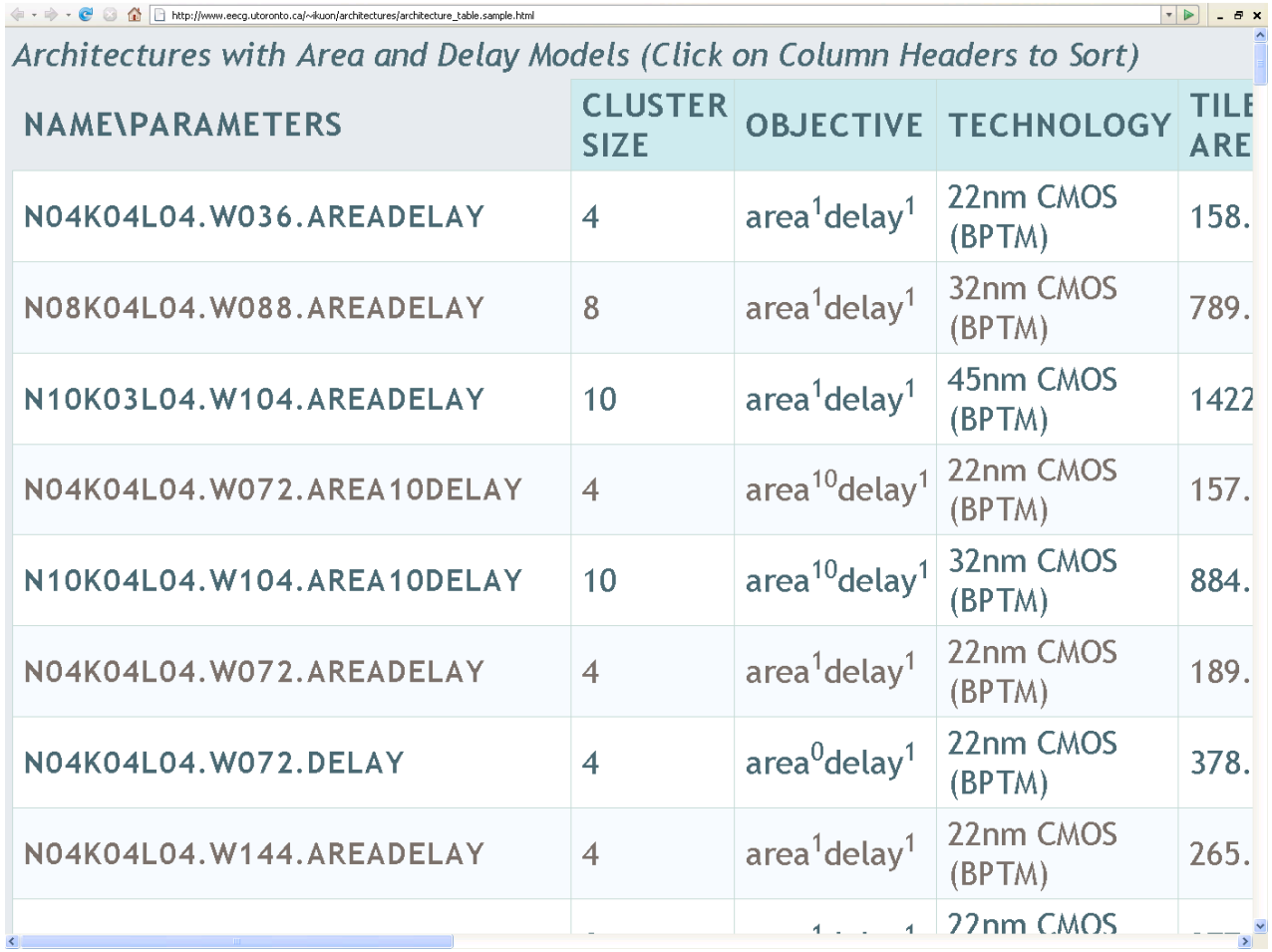
VPR 5.0 New Features

1. Single Driver Routing Architecture
   - Unidirectional/Direct Drive; dominates
   - [Virtex98] [Lewis03] [Lemieux04]
2. Heterogeneity
   - Can model different blocks types
3. **Wide Selection of Architecture Files**
   - **Transistor-Level Design Optimized;**
   - **Different Area/Speed Trade-offs**
   - **IC process down to 22nm, based on PTM**
4. Regression Test Suite
   - To maintain robustness





Architecture Repository for VPR



Architectures with Area and Delay Models (Click on Column Headers to Sort)

NAME\PARAMETERS	CLUSTER SIZE	OBJECTIVE	TECHNOLOGY	TILE ARE
N04K04L04.W036.AREADELAY	4	$area^{1}delay^{1}$	22nm CMOS (BPTM)	158.
N08K04L04.W088.AREADELAY	8	$area^{1}delay^{1}$	32nm CMOS (BPTM)	789.
N10K03L04.W104.AREADELAY	10	$area^{1}delay^{1}$	45nm CMOS (BPTM)	1422
N04K04L04.W072.AREA10DELAY	4	$area^{10}delay^{1}$	22nm CMOS (BPTM)	157.
N10K04L04.W104.AREA10DELAY	10	$area^{10}delay^{1}$	32nm CMOS (BPTM)	884.
N04K04L04.W072.AREADELAY	4	$area^{1}delay^{1}$	22nm CMOS (BPTM)	189.
N04K04L04.W072.DELAY	4	$area^{0}delay^{1}$	22nm CMOS (BPTM)	378.
N04K04L04.W144.AREADELAY	4	$area^{1}delay^{1}$	22nm CMOS (BPTM)	265.
			22nm CMOS	

VPR 5.0 – More Information

- More details, documentation and Beta of VPR 5.0 at:

  http://www.eecg.utoronto.ca/vpr

- Talk to me, Jonathan Rose, or Jason Luu

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