Dynamic Hazard Resolution for Pipelining Irregular Loops in High-Level Synthesis

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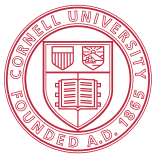
[2] Computer Science, Harvard University



Cornell University

CSL

Loop Pipelining in High-Level Synthesis

- Ultimate Goal
  - Synthesize an efficient pipeline with the highest possible throughput for all kinds of applications
- Conventional HLS pipelining
  - Ineffective for loops with data-dependent memory accesses
    - Cannot be predicted by static compiler analysis
    - Infrequent dynamic structural and data hazards
- Our Study
  - Augment HLS synthesized pipeline with application-specific dynamic hazard resolution logic

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Pipelining Loops with Infrequent Hazards

Maximal Matching

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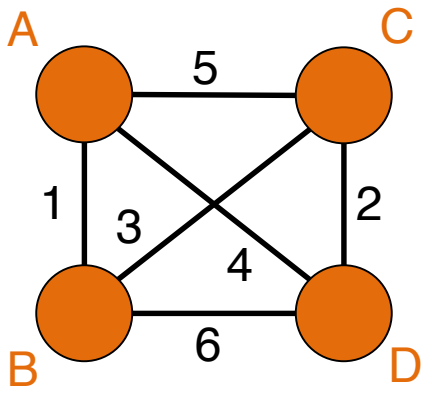

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Clock Cycles

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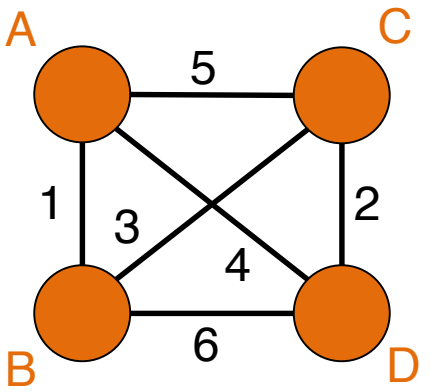

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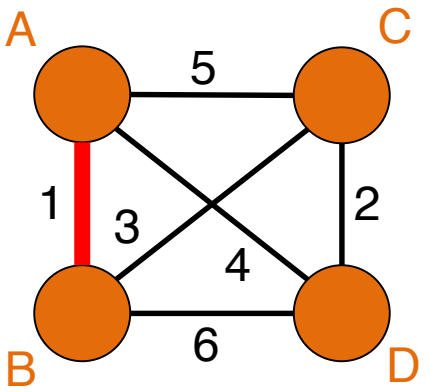

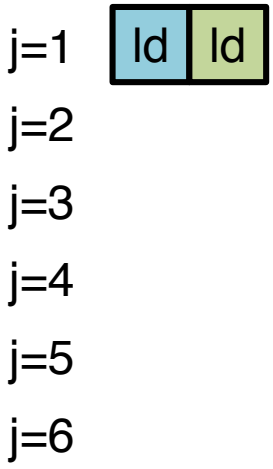

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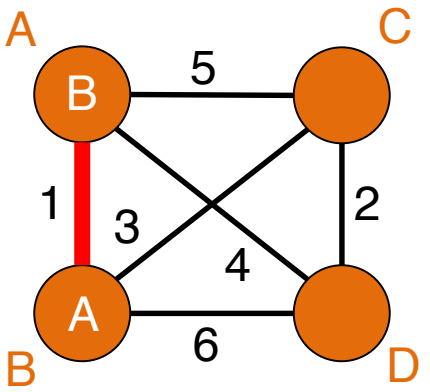

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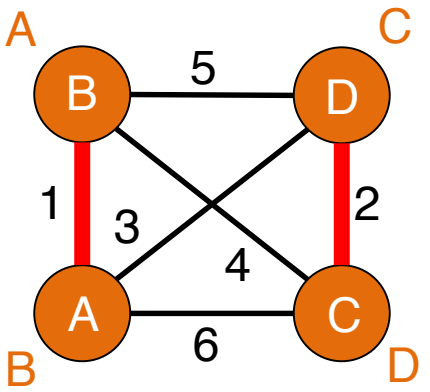

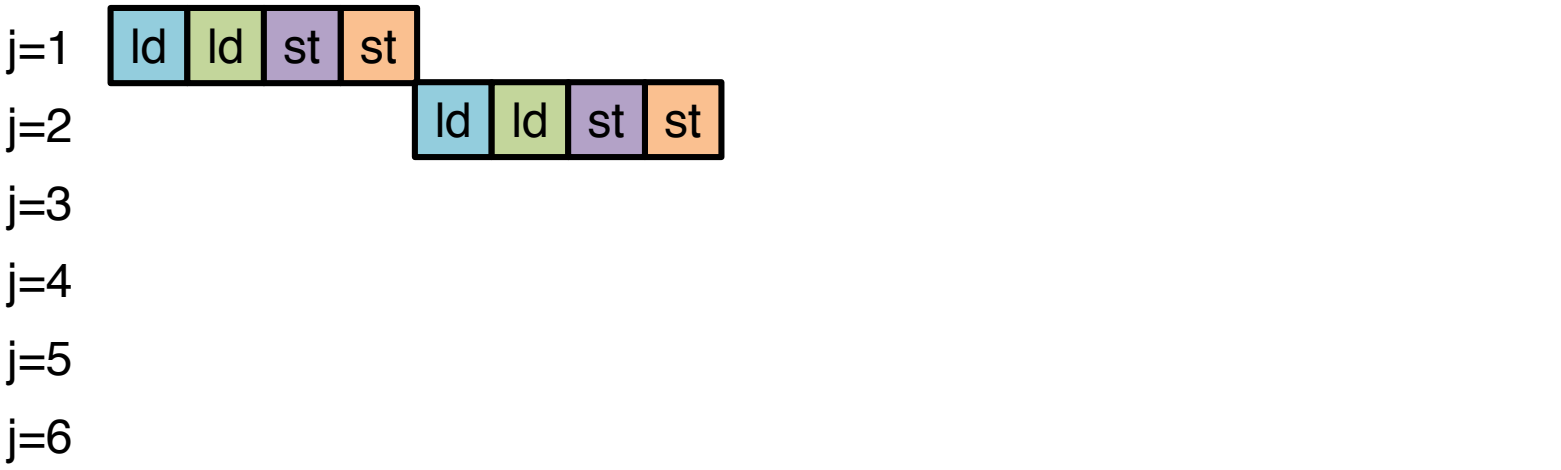

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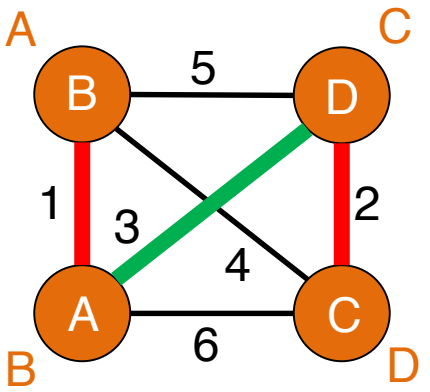

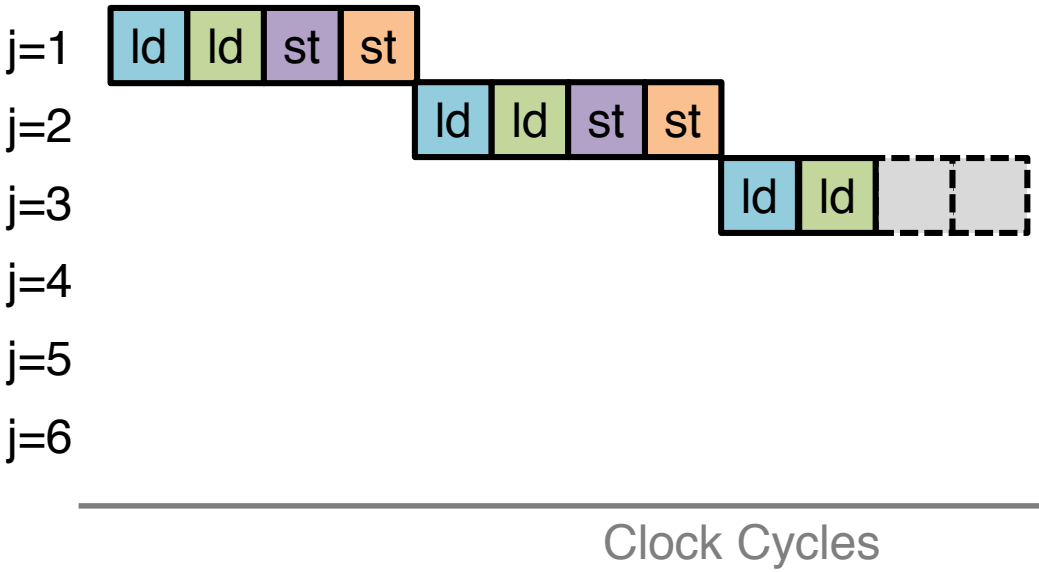

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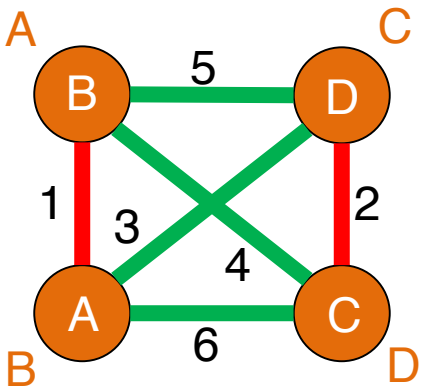

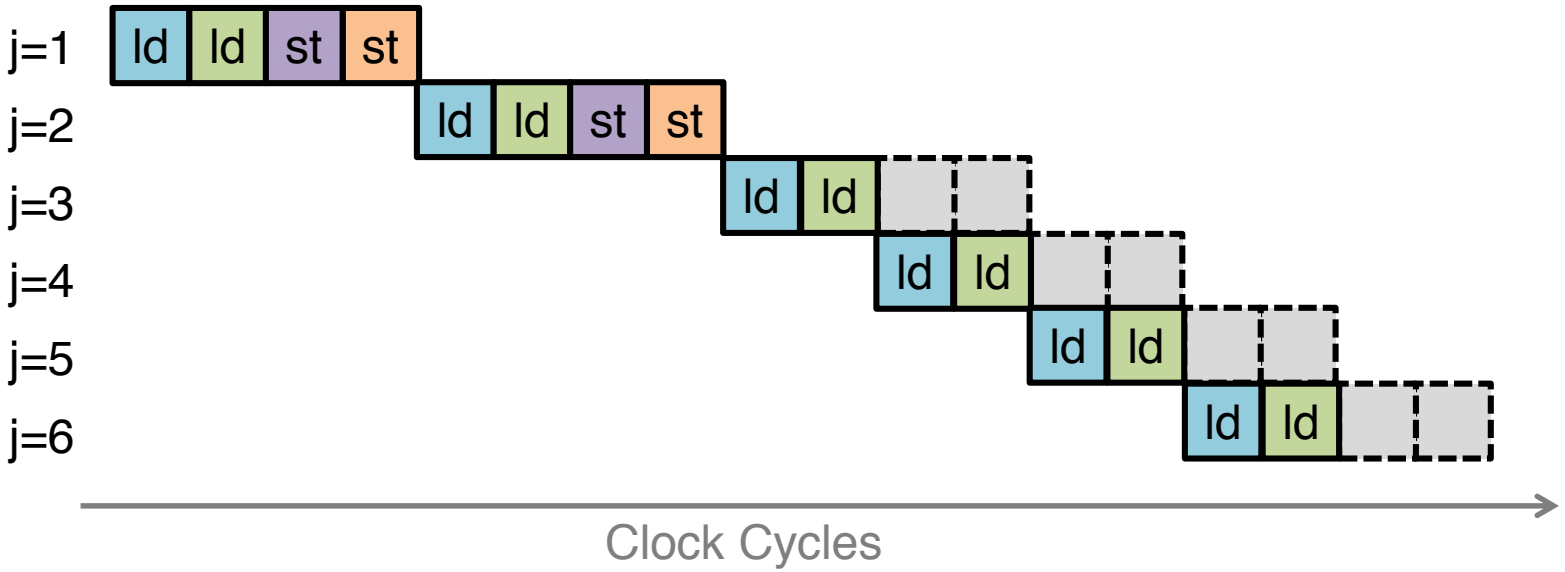

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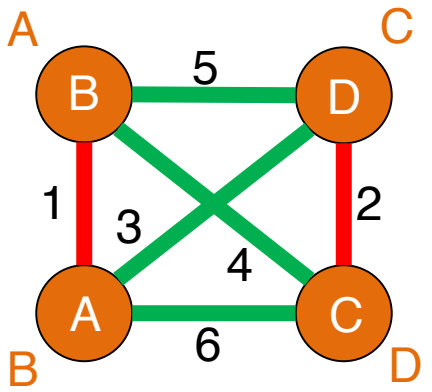
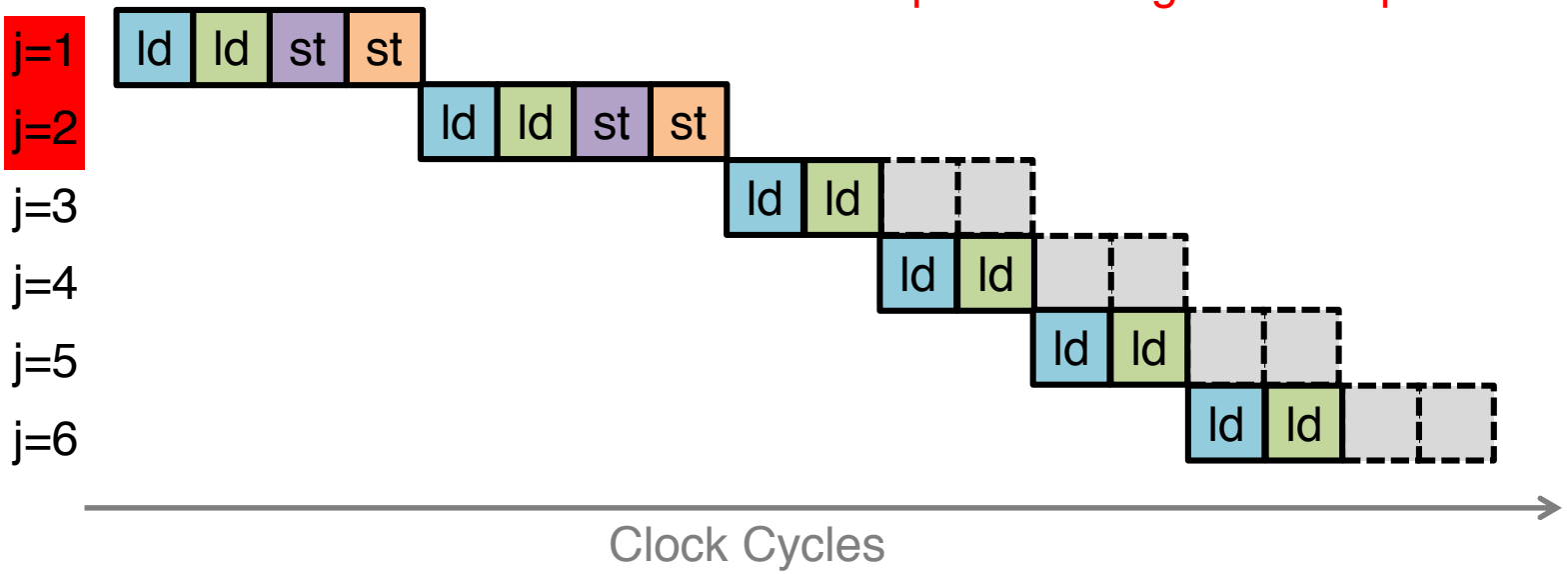


Independent edges → Requires stores



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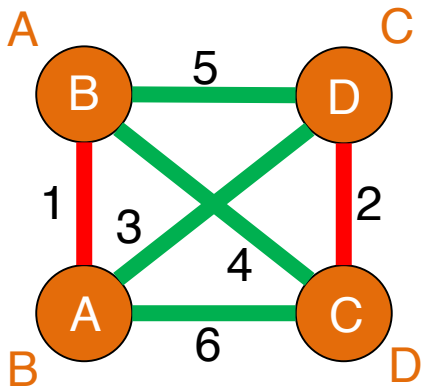
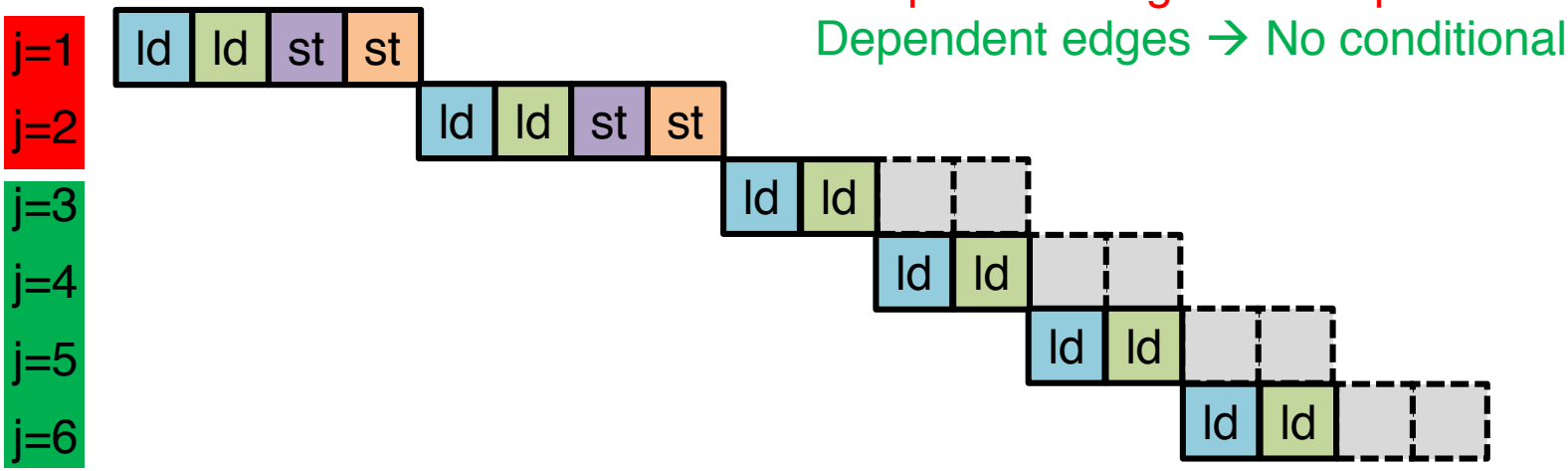


Independent edges → Requires stores

Dependent edges → No conditional stores



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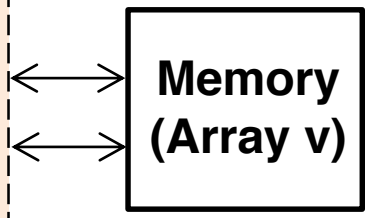

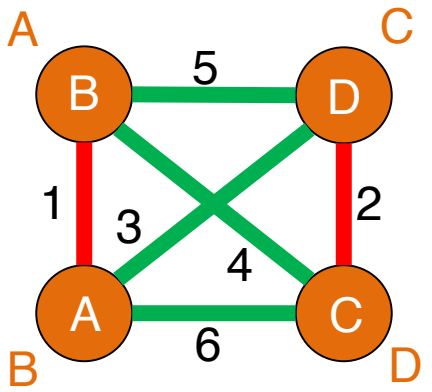

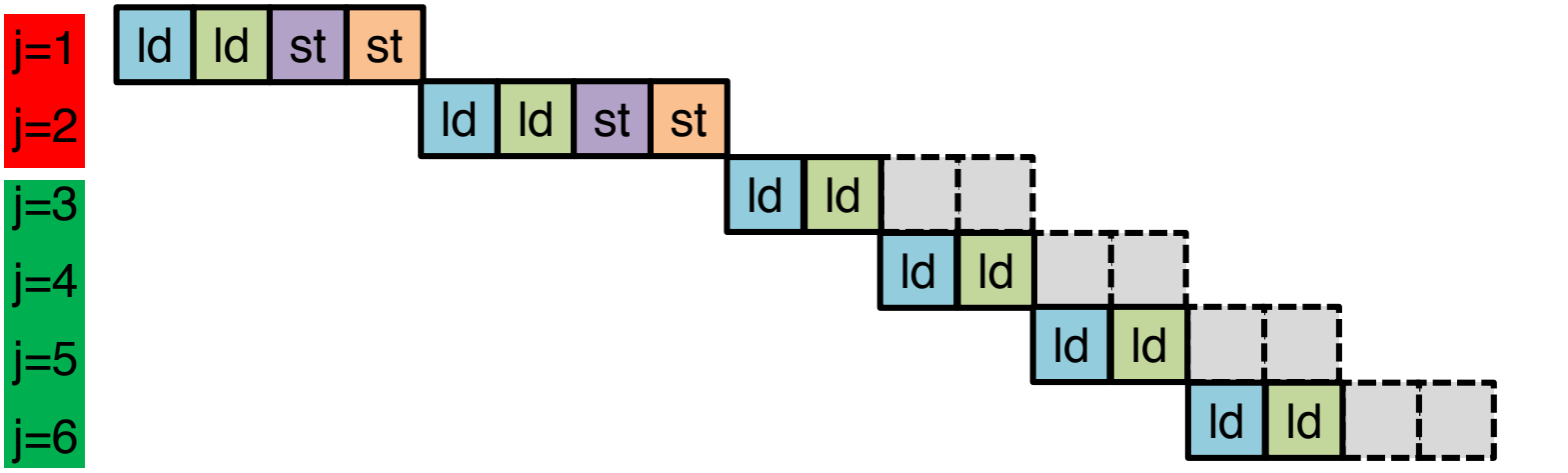

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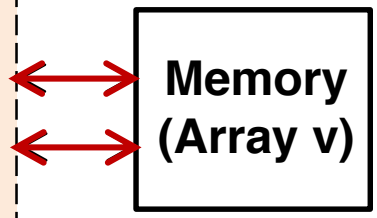
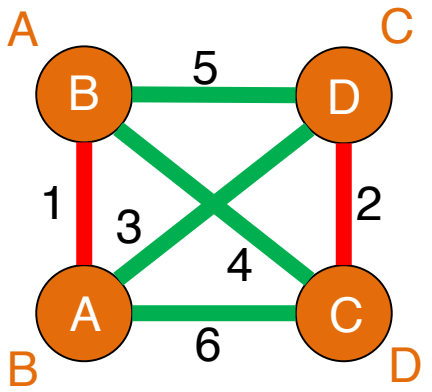
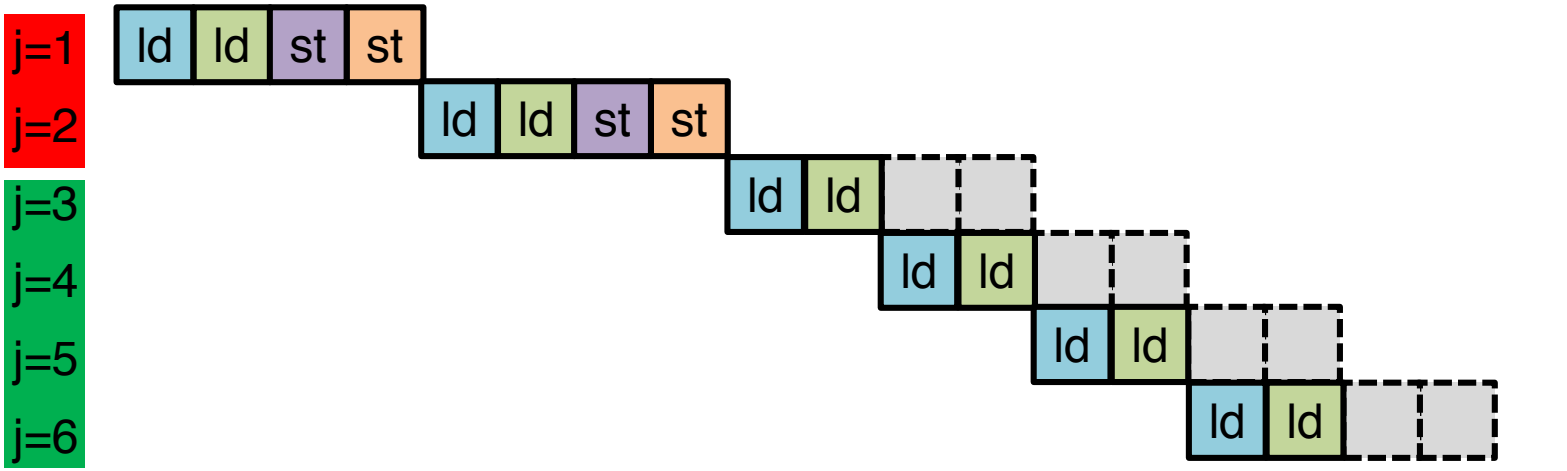
structural hazards (memory ports)







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Memory (Array v)

Data hazards (read-after-write)

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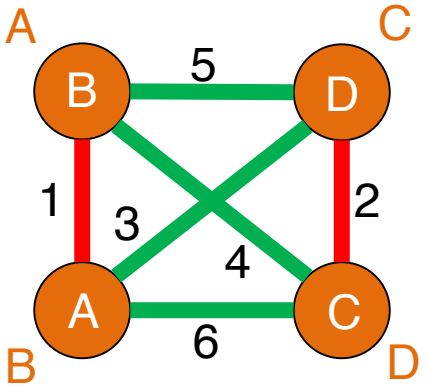

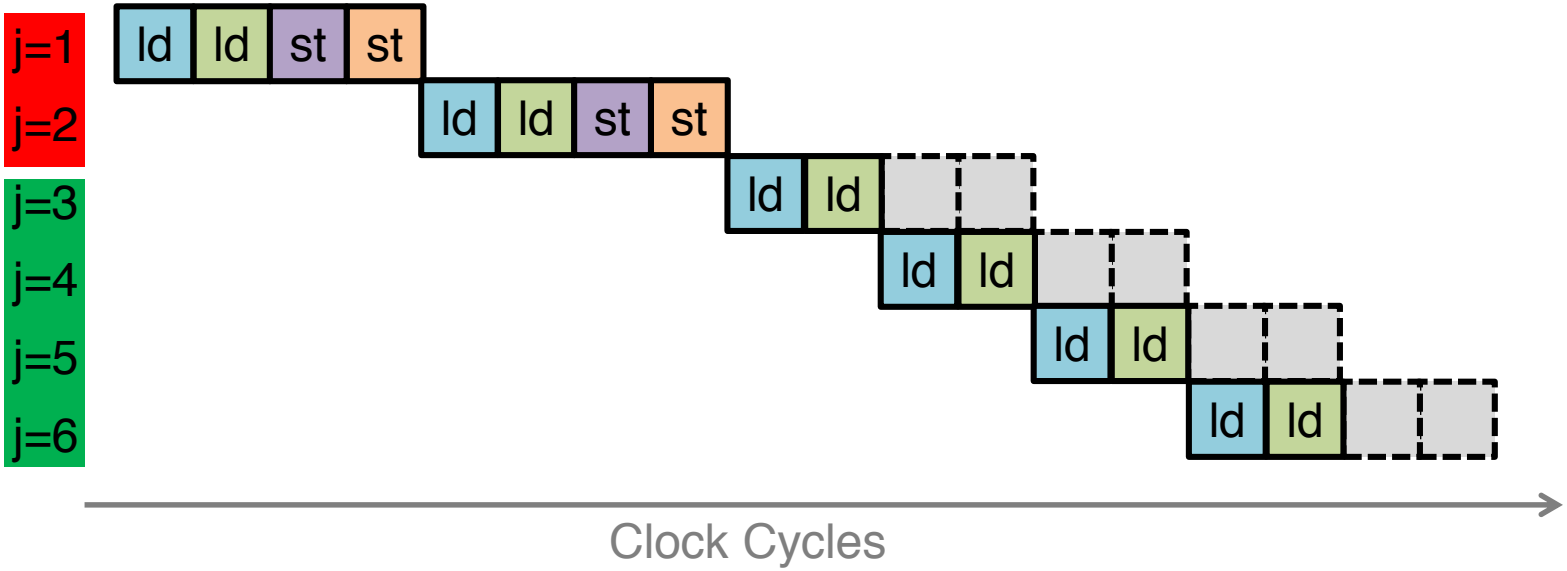

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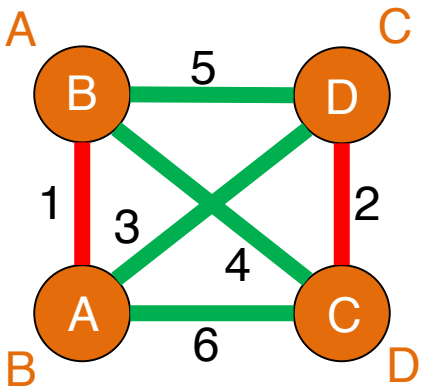
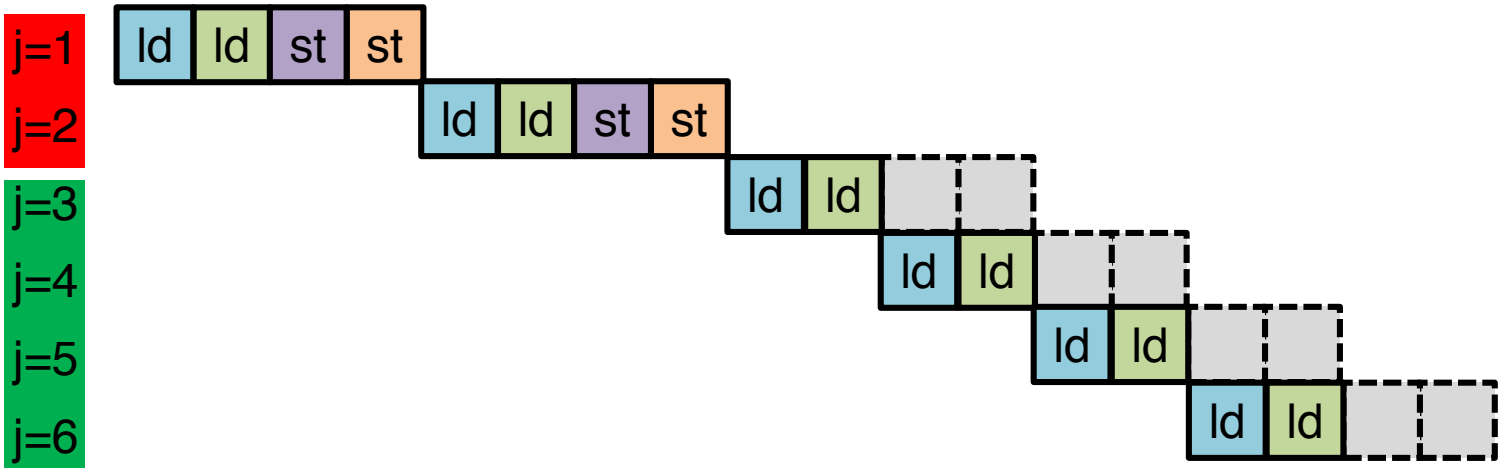
Occur infrequently





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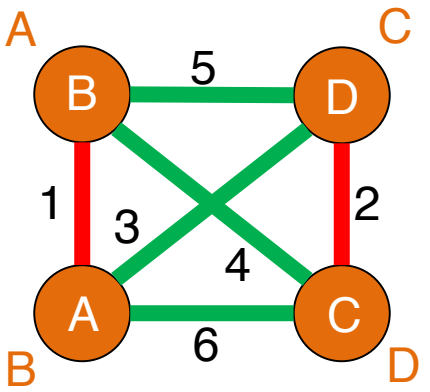
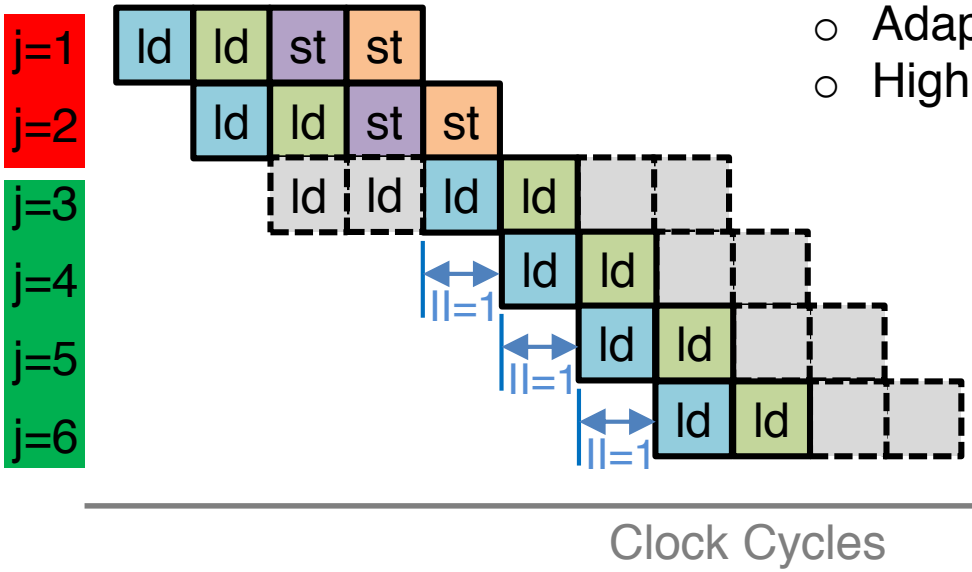


Optimal Schedule

- Adapts to dynamic infrequent hazards
- High throughput for most iterations



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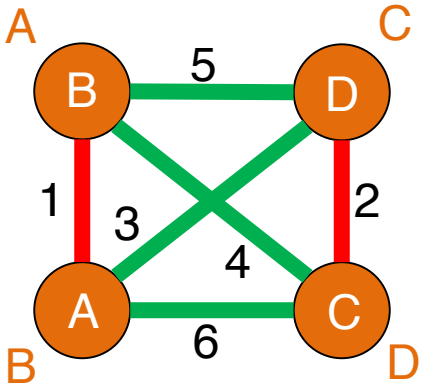

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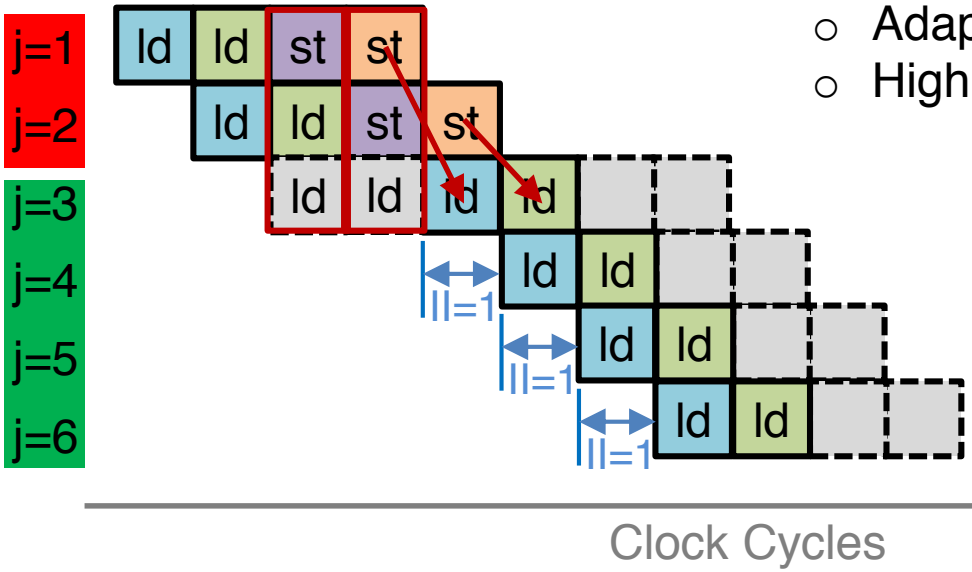

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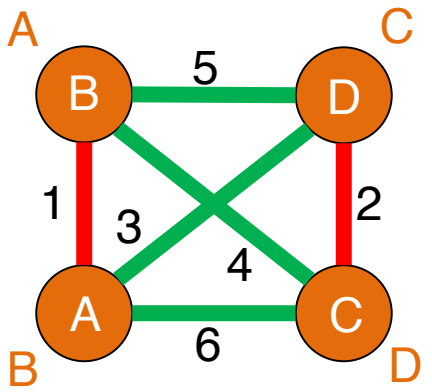
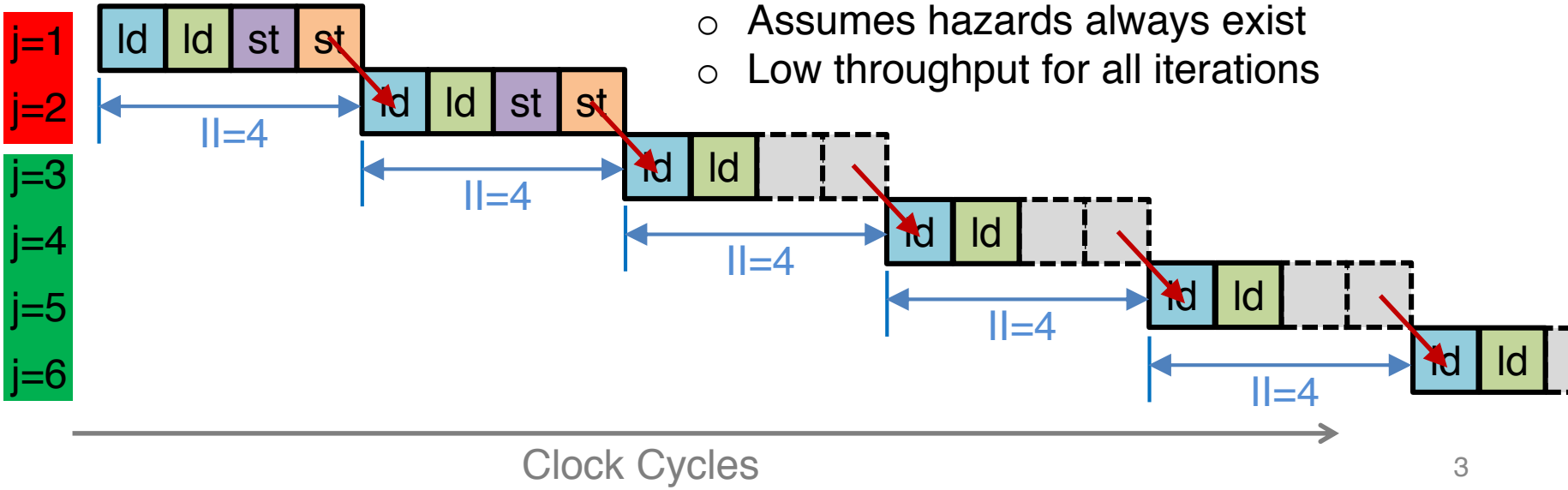


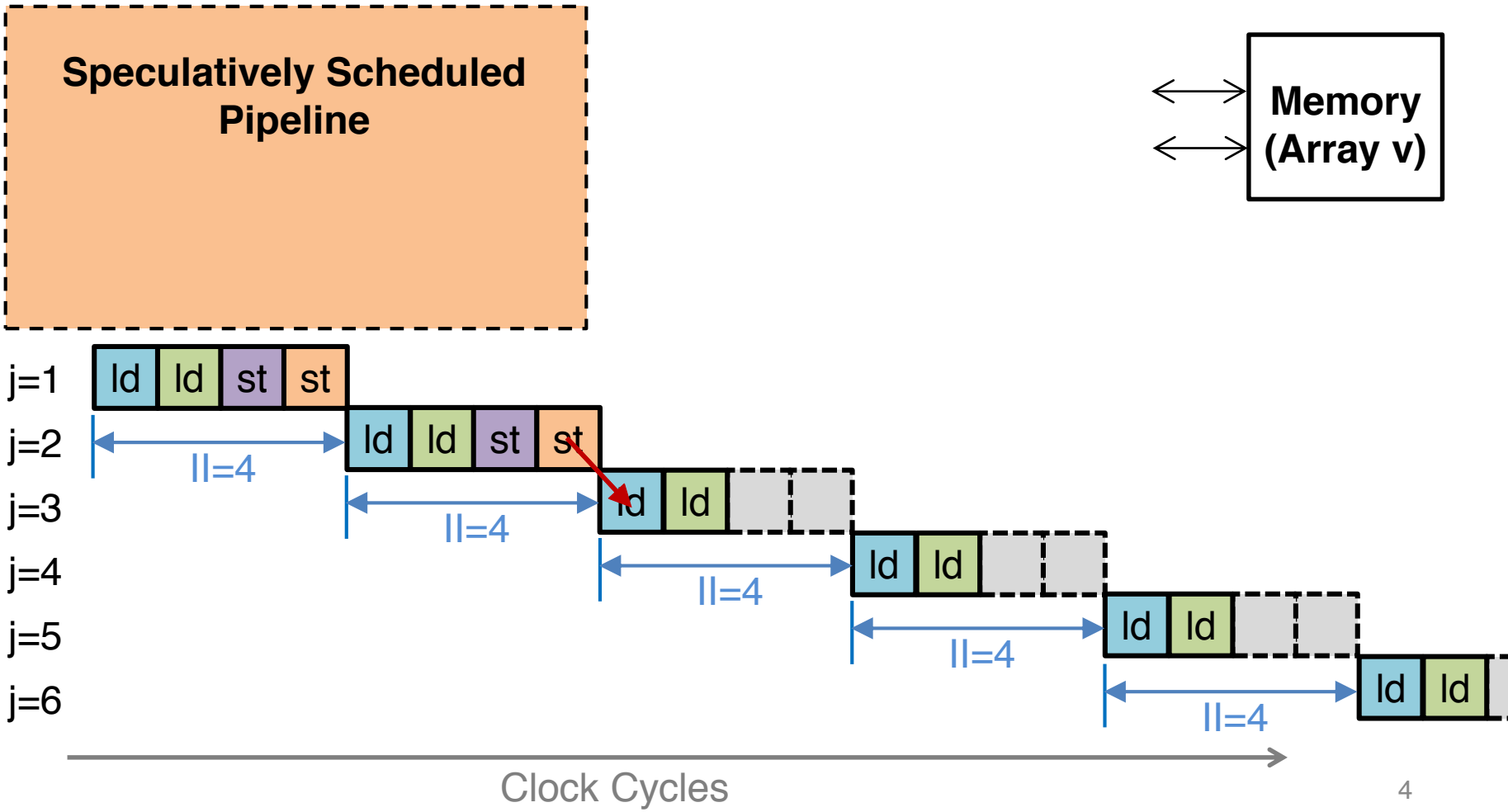
Conventional HLS Schedule

- Assumes hazards always exist
- Low throughput for all iterations



Dynamic Hazard Resolution for HLS

- Create a speculative pipeline for common case and rely on hazard resolution units to resolve hazards at runtime



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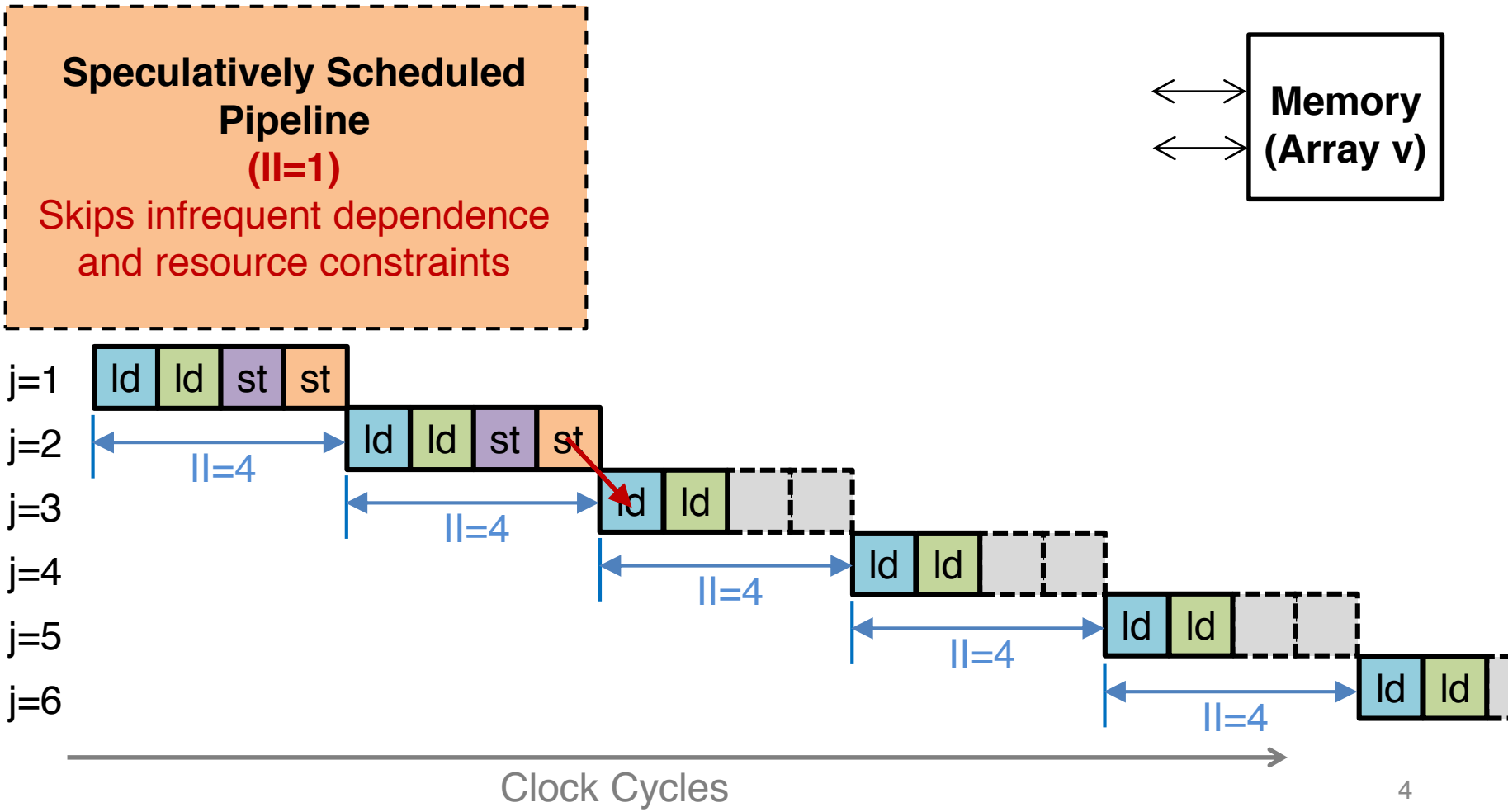

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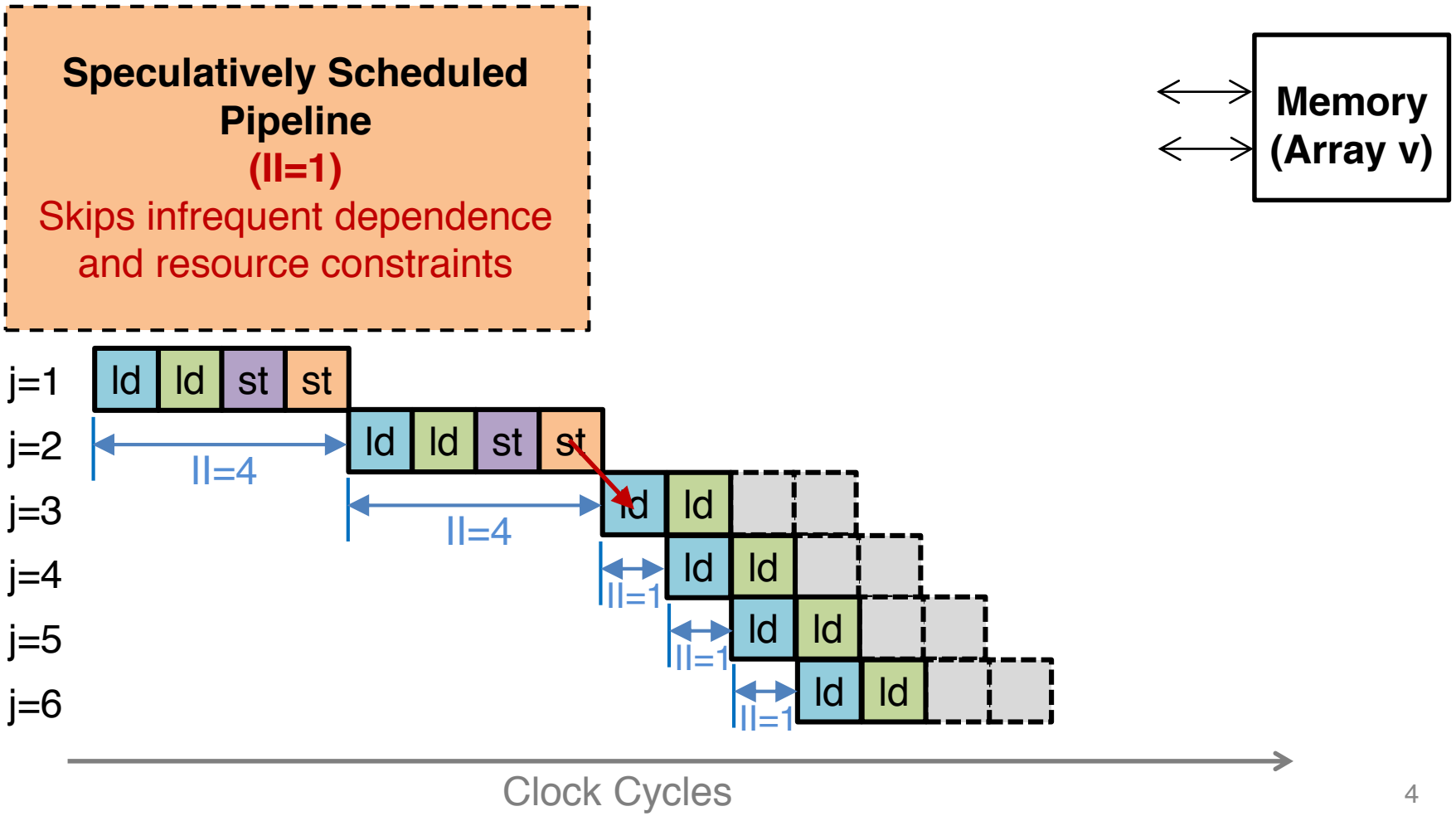

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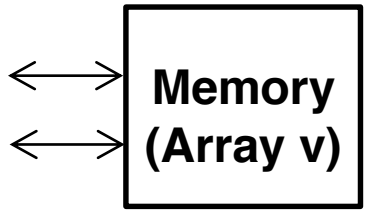
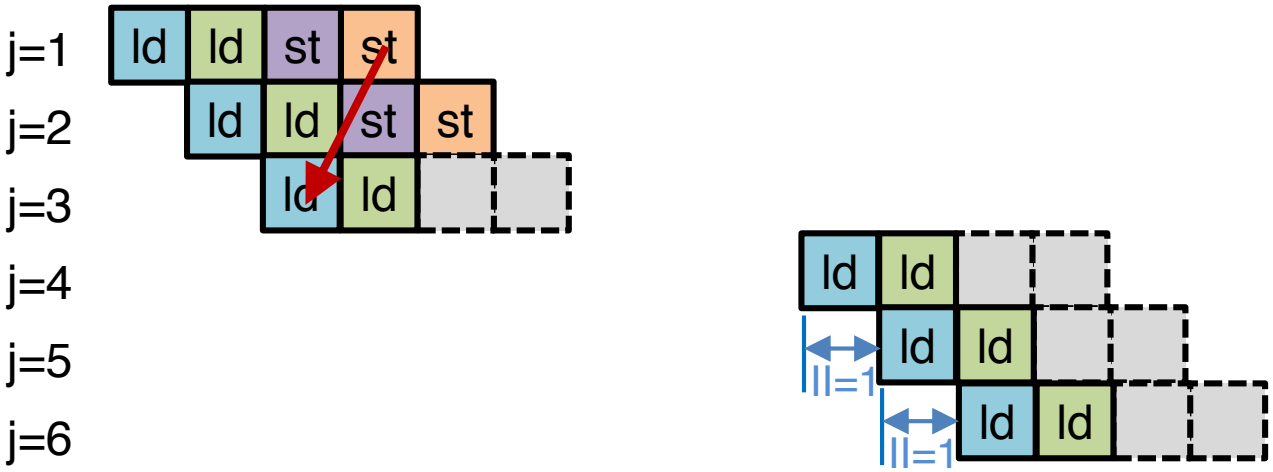
Speculatively Scheduled Pipeline
(II=1)
Skips infrequent dependence and resource constraints





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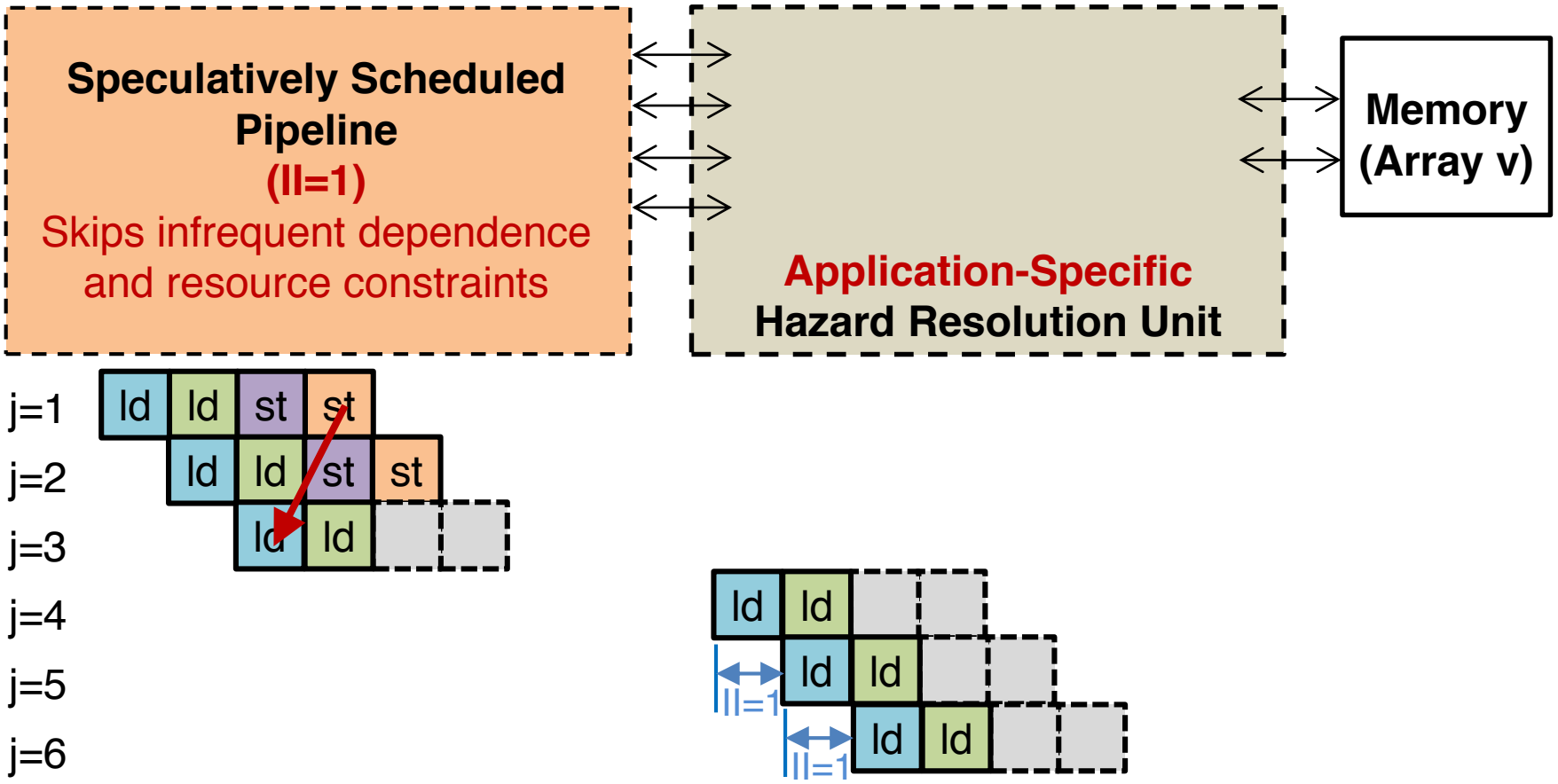

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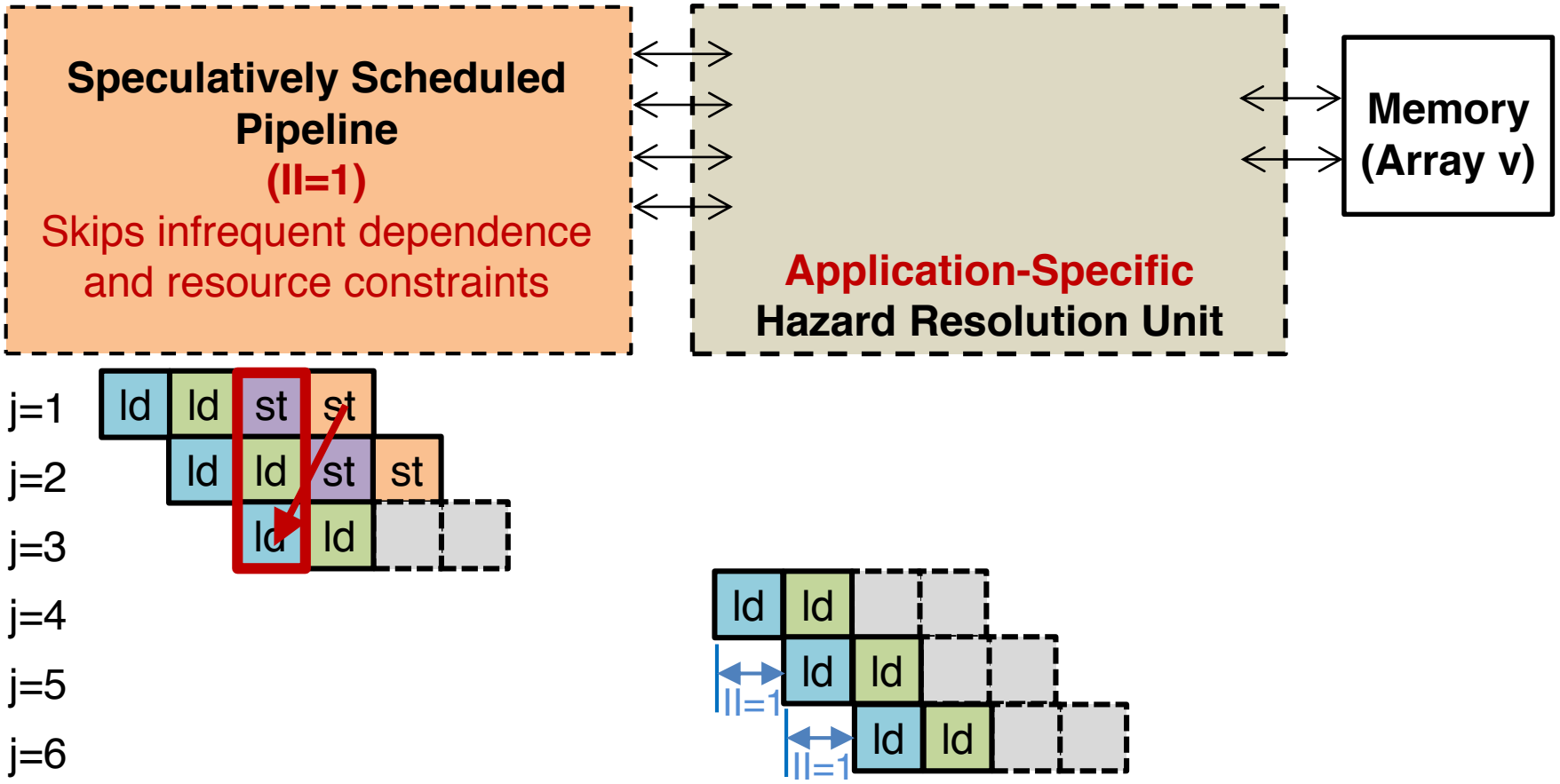

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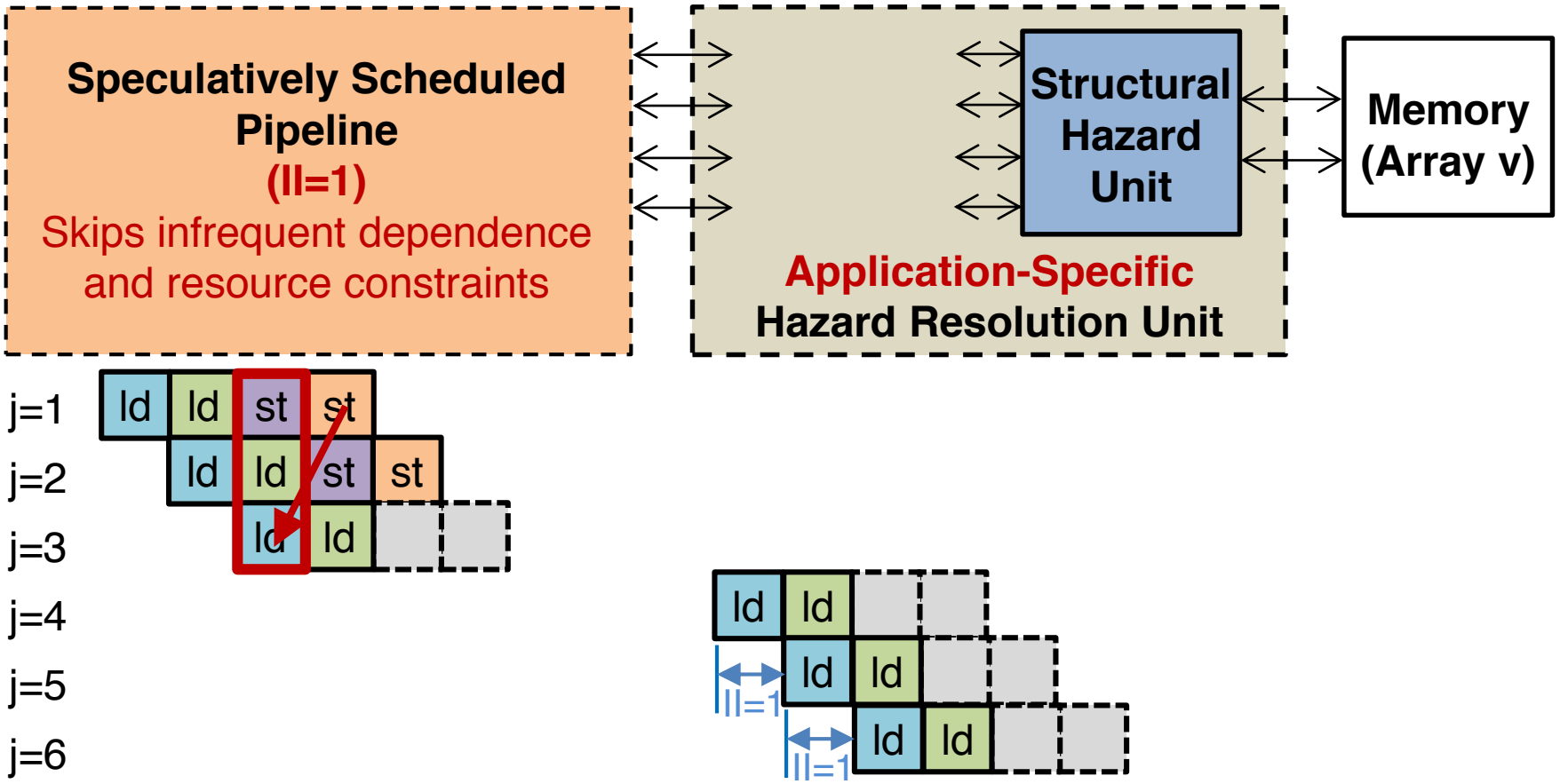

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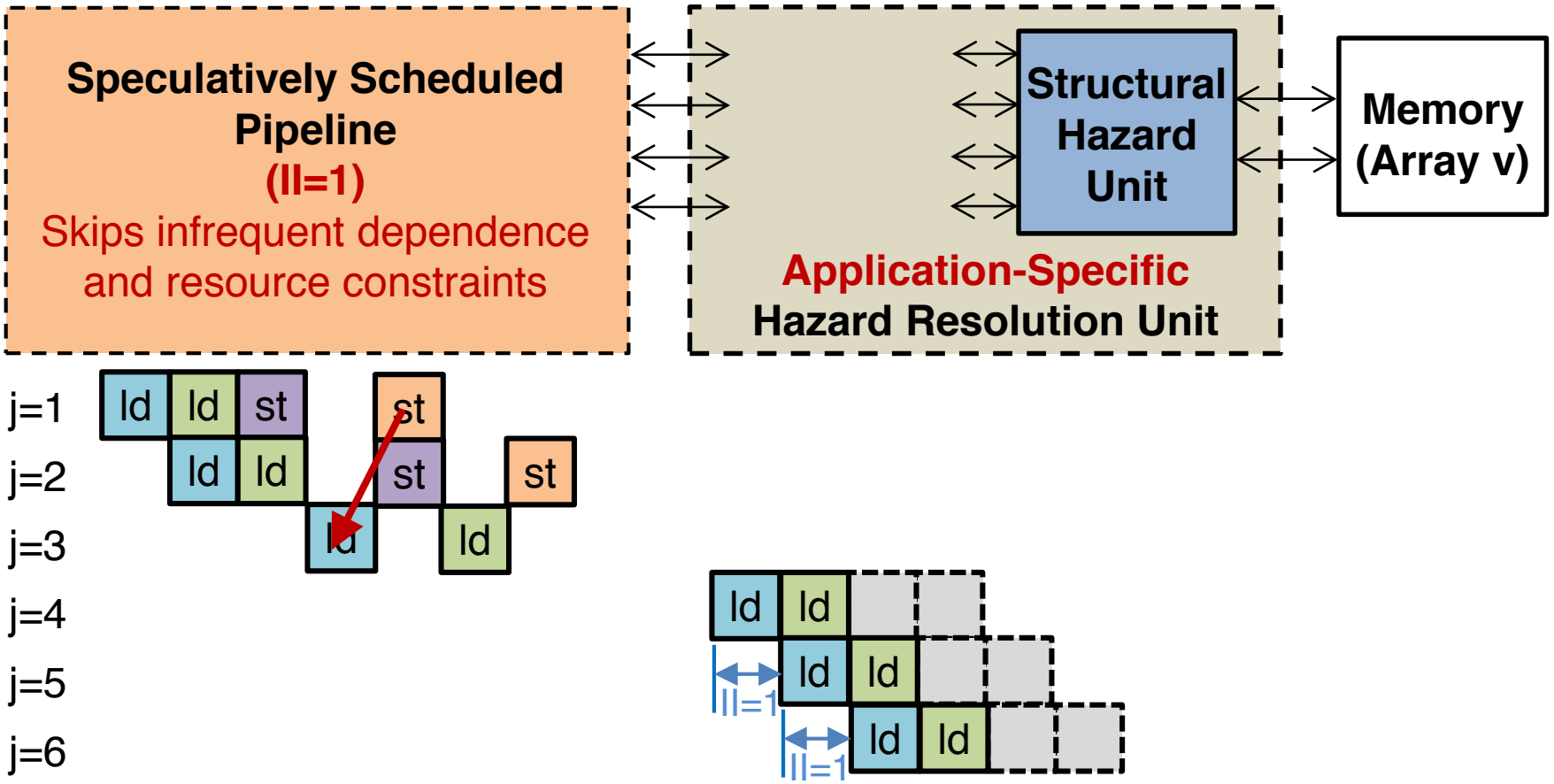

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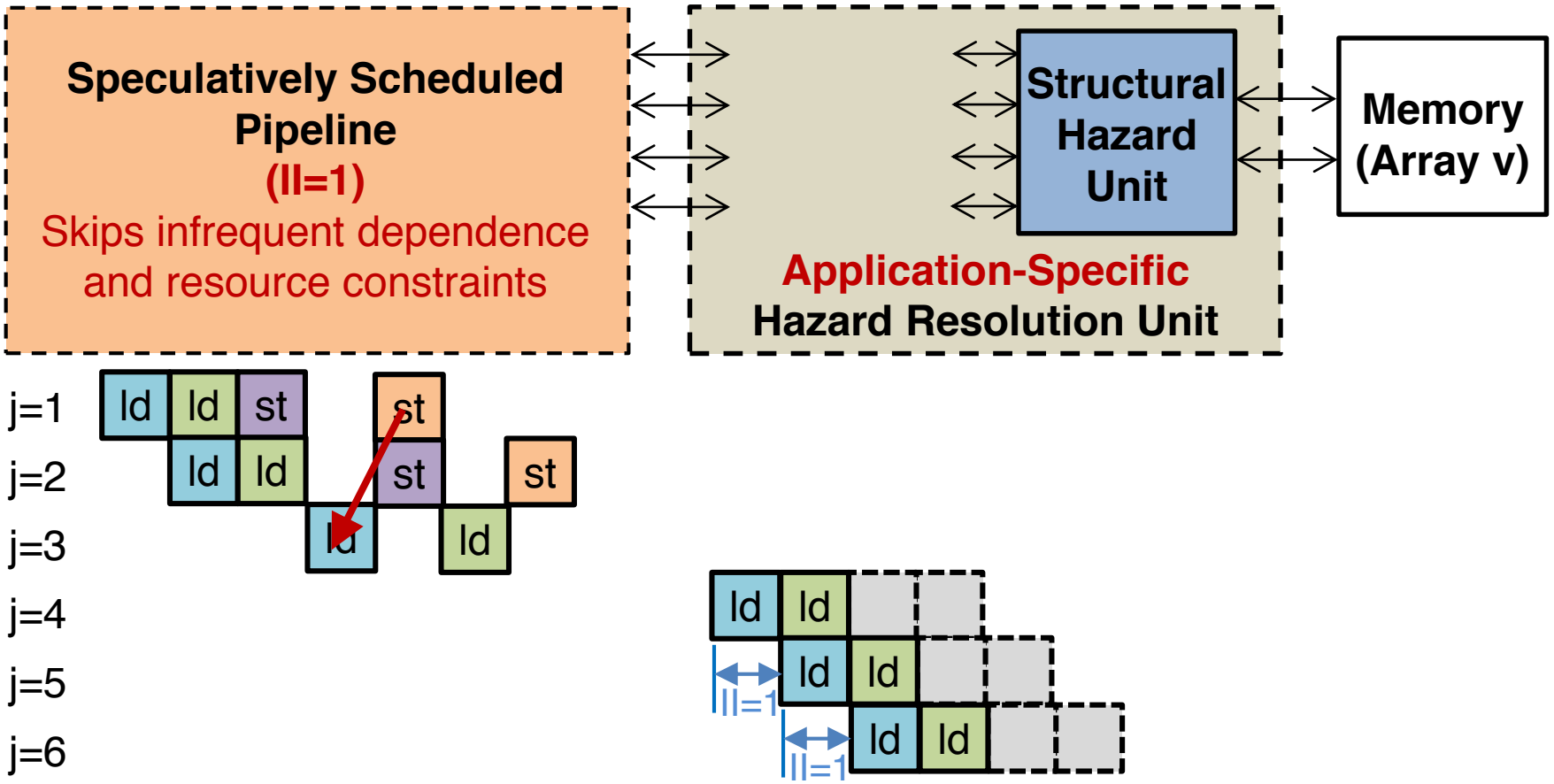

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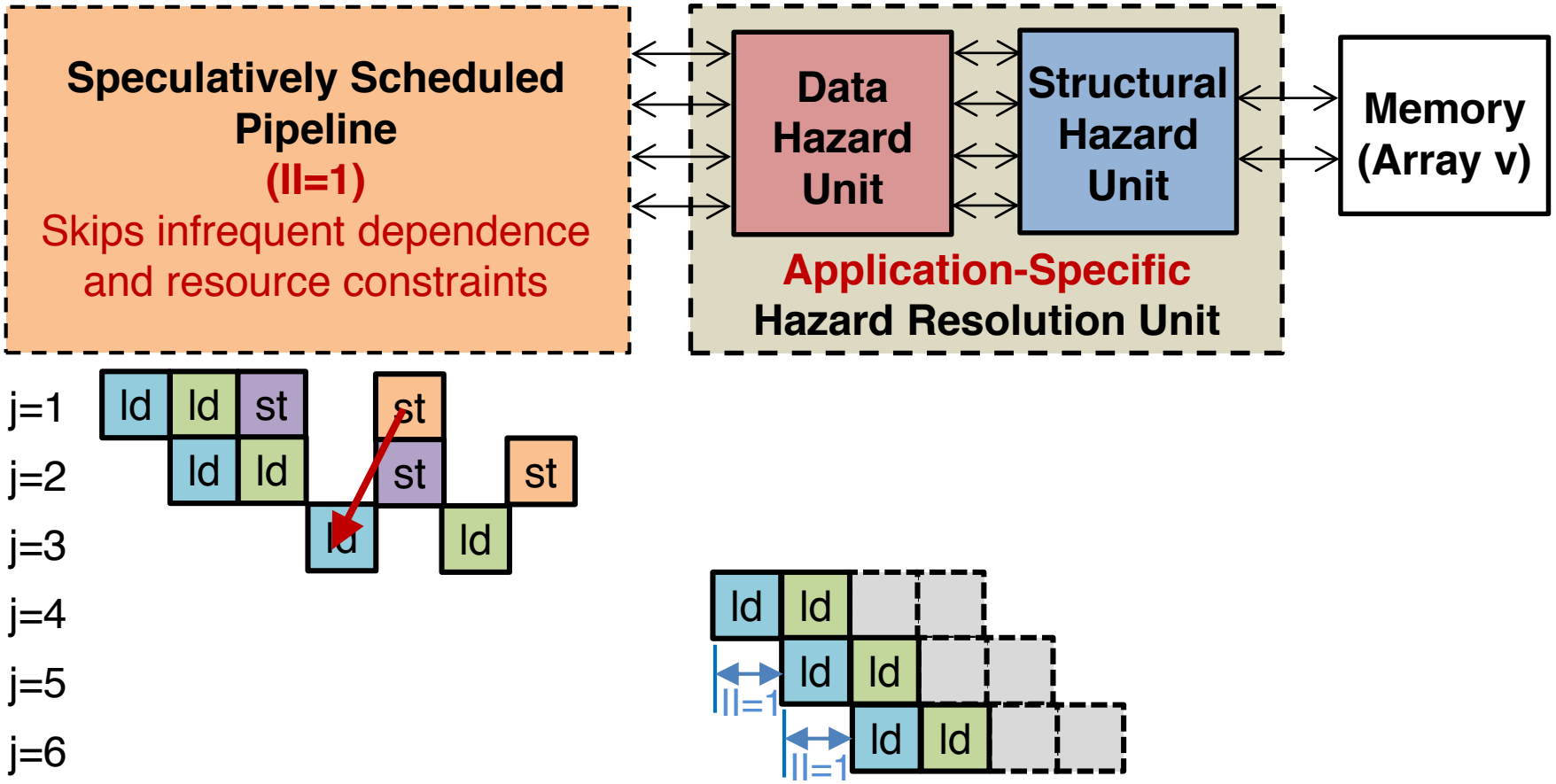

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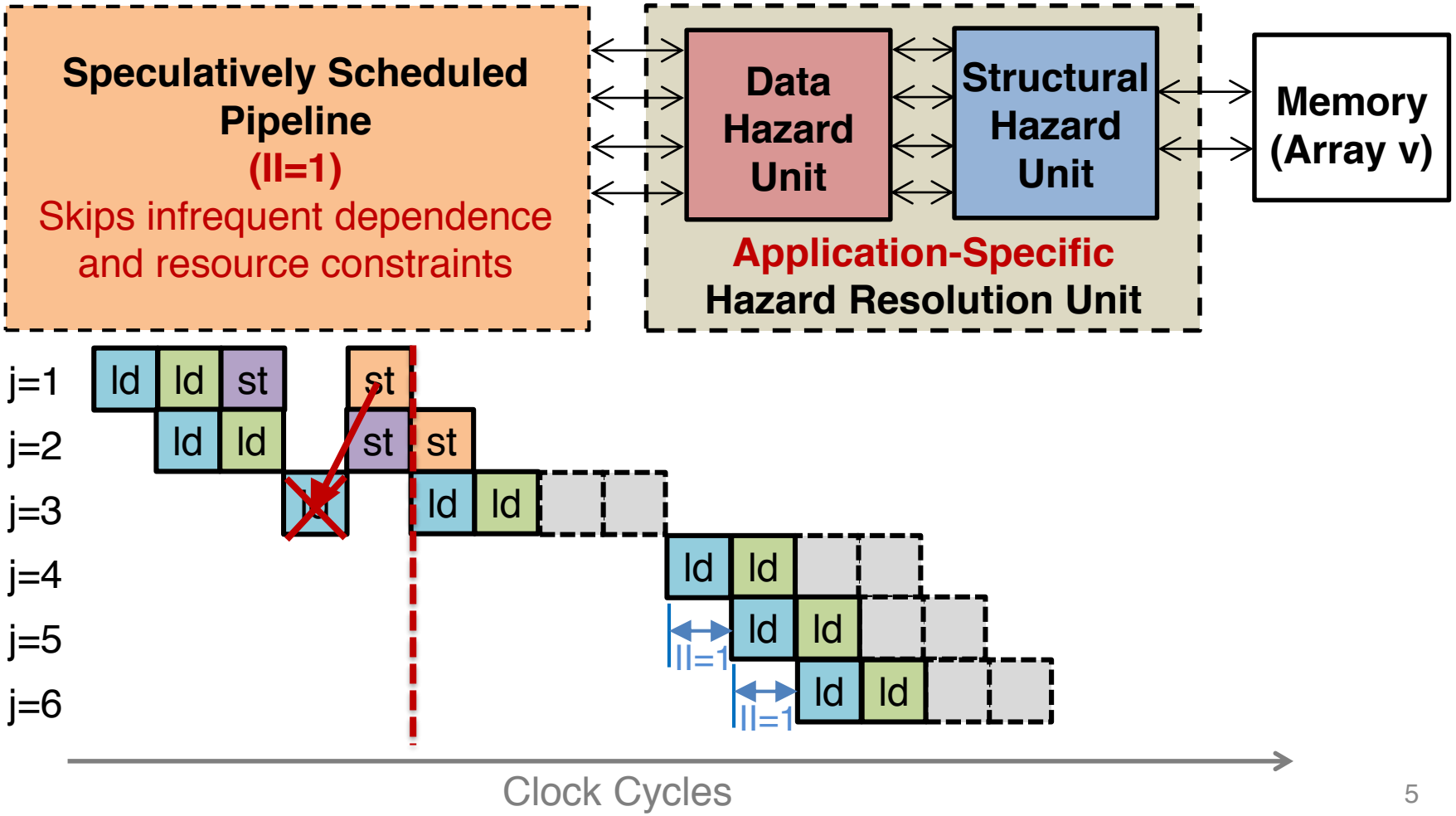

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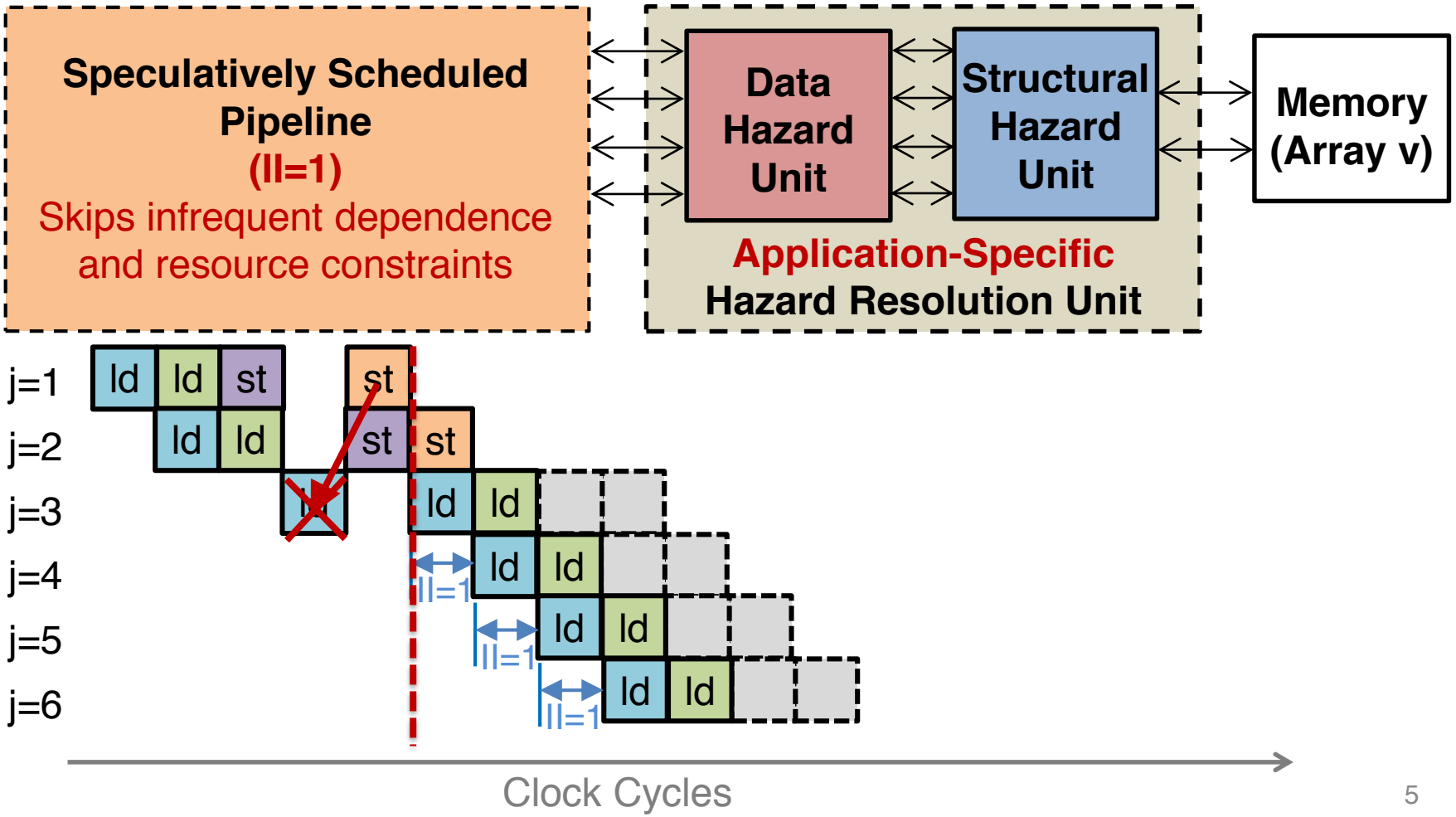
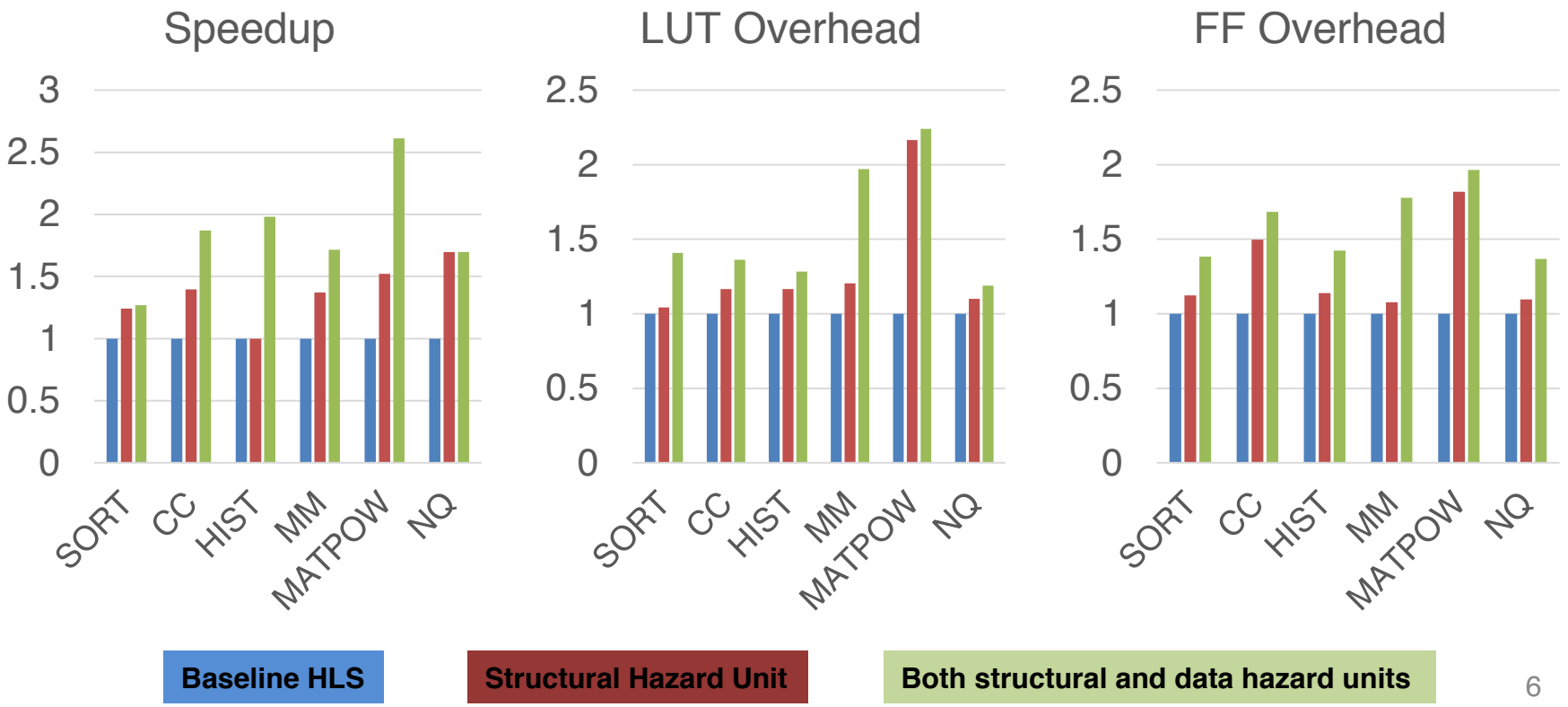


Experimental Results

- Significant speedup with reasonable area overhead
  - Amount of speedup depends on input pattern, data access pattern, and available memory bandwidth
  - Tradeoff between performance gain and hazard logic overhead



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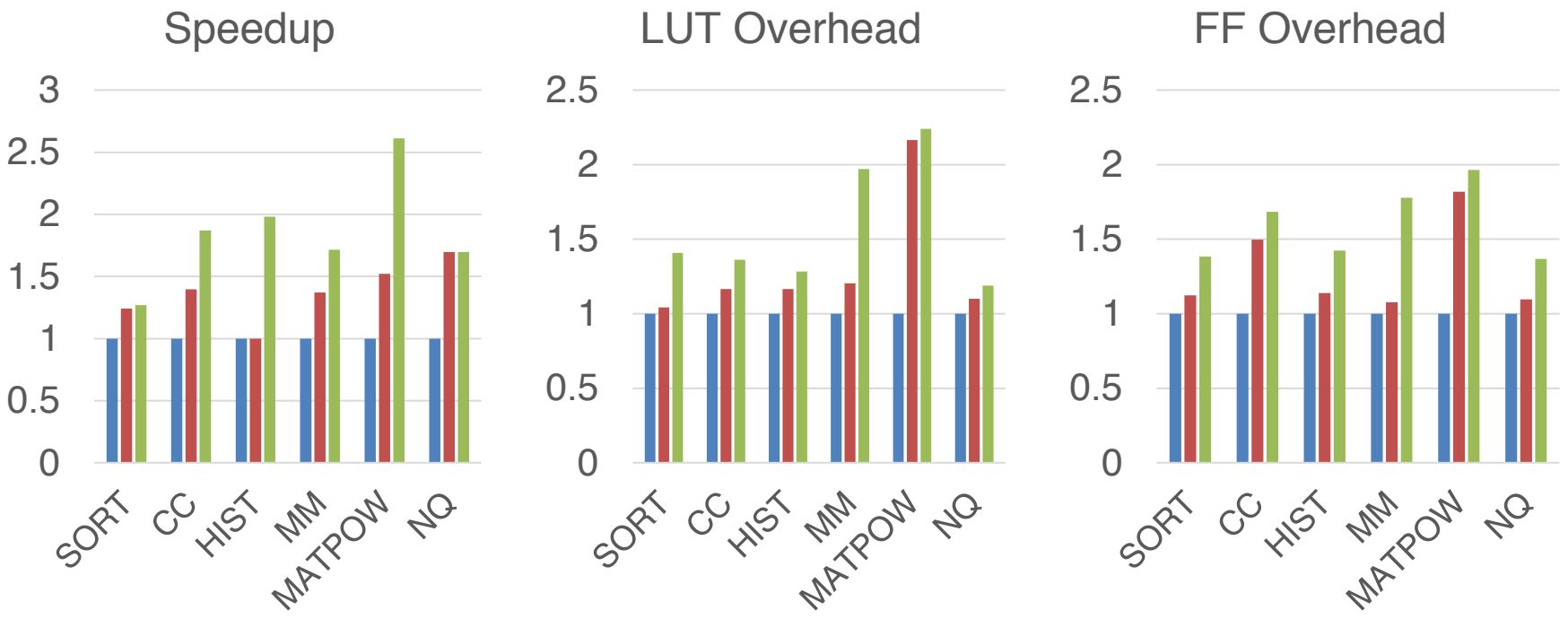

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