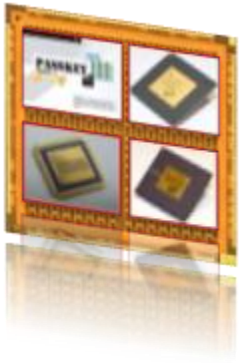
NAND-NOR :
A Compact, Fast, and Delay Balanced FPGA Logic Element

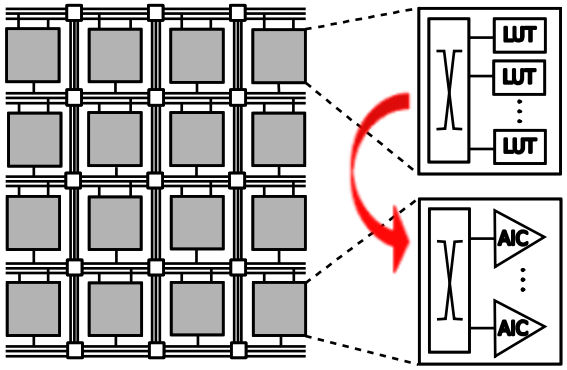
Zhihong Huang†, Xing Wei †, Grace Zgheib‡, Wei Li †, Yu Lin†,
Zhenghong Jiang †, Kaihui Tu†, Paolo Ienne‡, Haigang Yang †

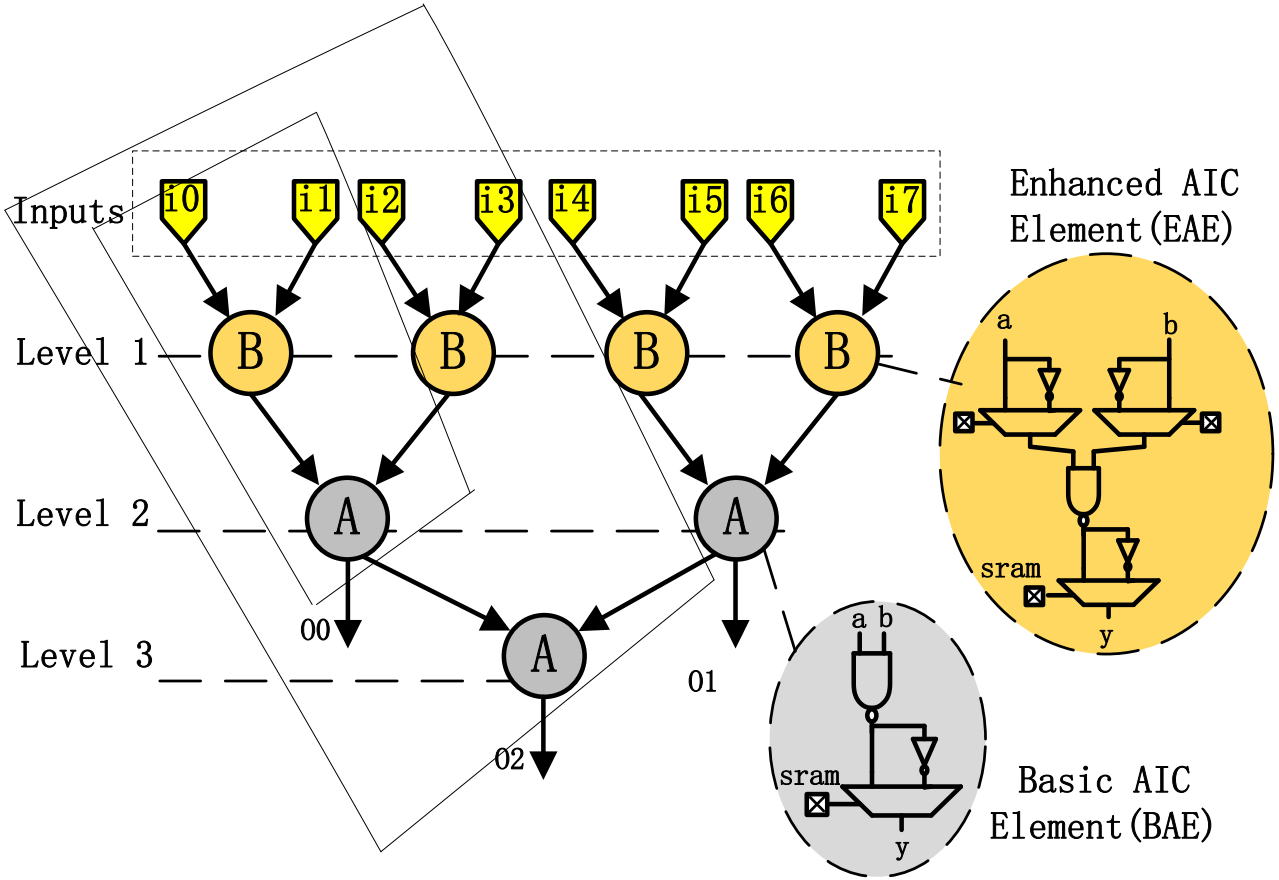


† Institute of Electronics, Chinese Academy of Sciences (IECAS)
‡ Ecole Polytechnique Fédérale de Lausanne (EPFL)

AIC cone

- AND-INVETER-CONE (AIC), another possible logic element architecture compared to LUT

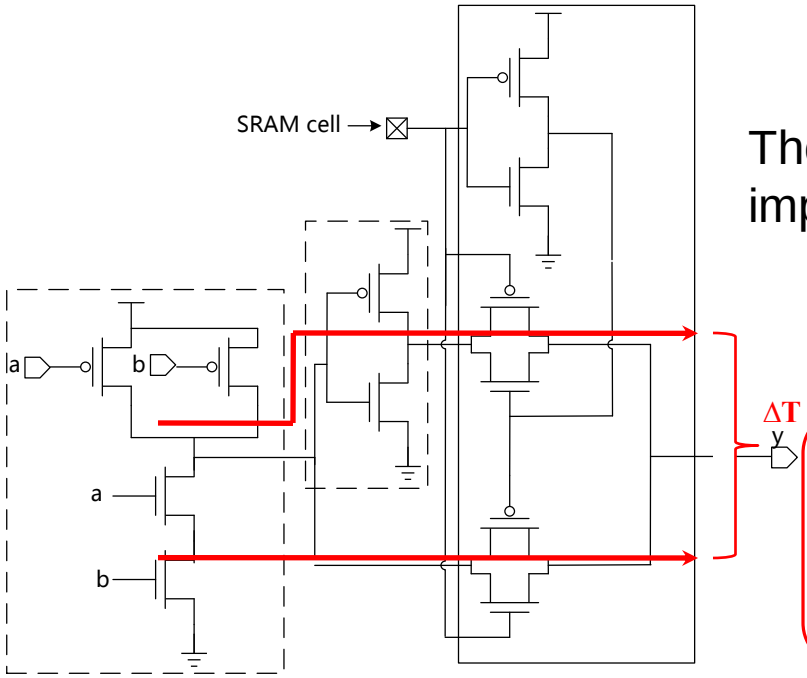




A 3-level AIC (AIC3) with its two types of nodes:
Enhanced AIC Element (EAE) and *Basic AIC Element* (BAE)

H. Parandeh-Afshar, G. Zgheib, D. Novo, M. Purnaprajna, and P. Ienne. Shadow And-Inverter Cones. In Proceedings of the 23rd International Conference on Field-Programmable Logic and Applications, pages 1-4, Porto, Portugal, Sept. 2013.

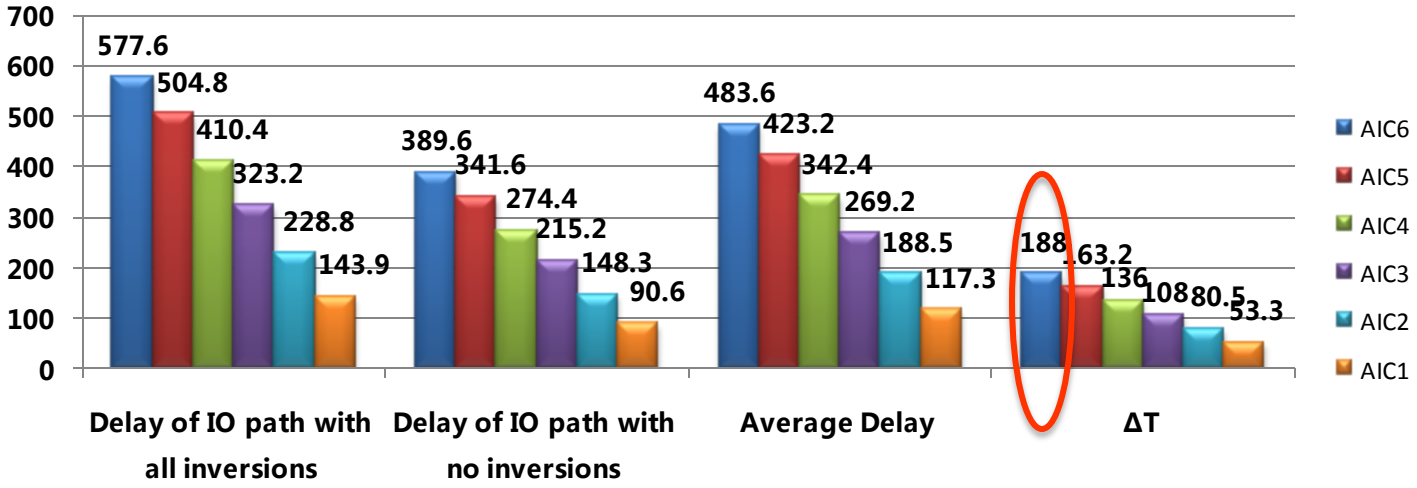
Delay discrepancy problem



The transistor-level implementation of a BAE

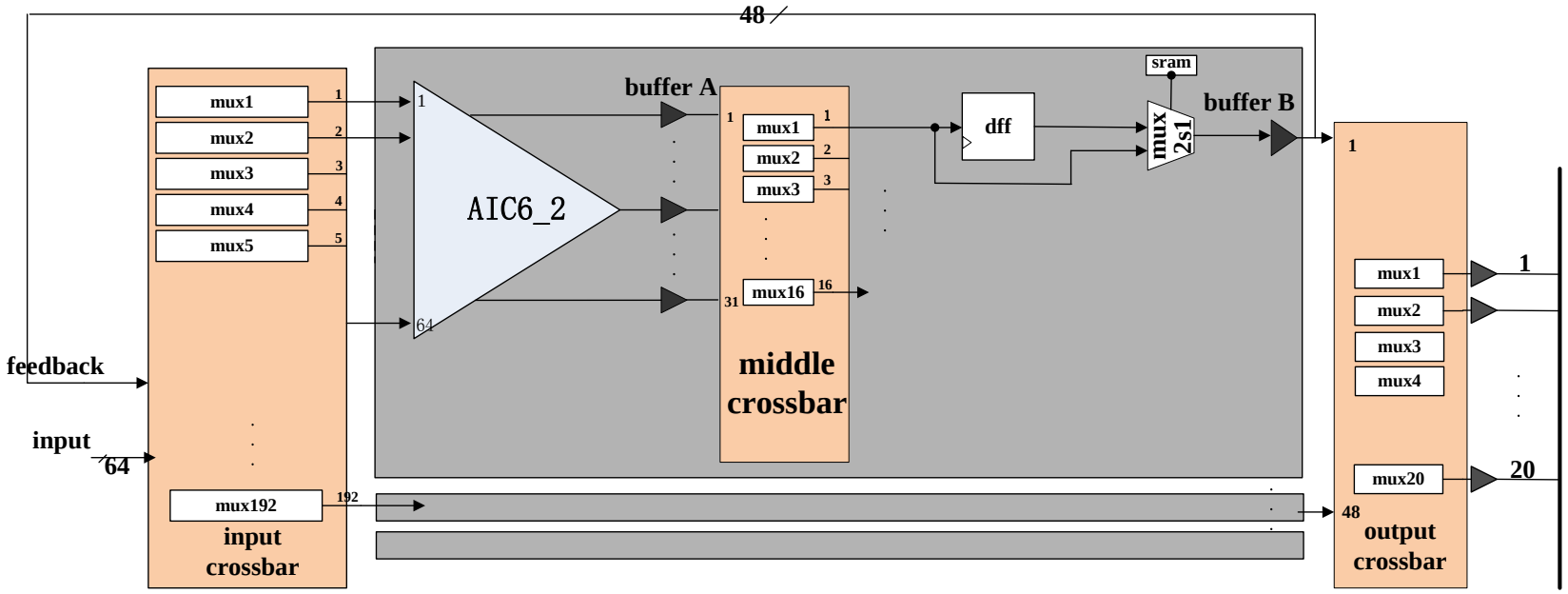
- Delay increases by about 50% when all the inversions as added, as opposed to none
- Further aggravated in the case of cascaded multilevel AICs

Delay of the AIC, with up to 6 levels, for both the best and worst-case scenarios (ps).



Inefficiency in existing AIC cluster

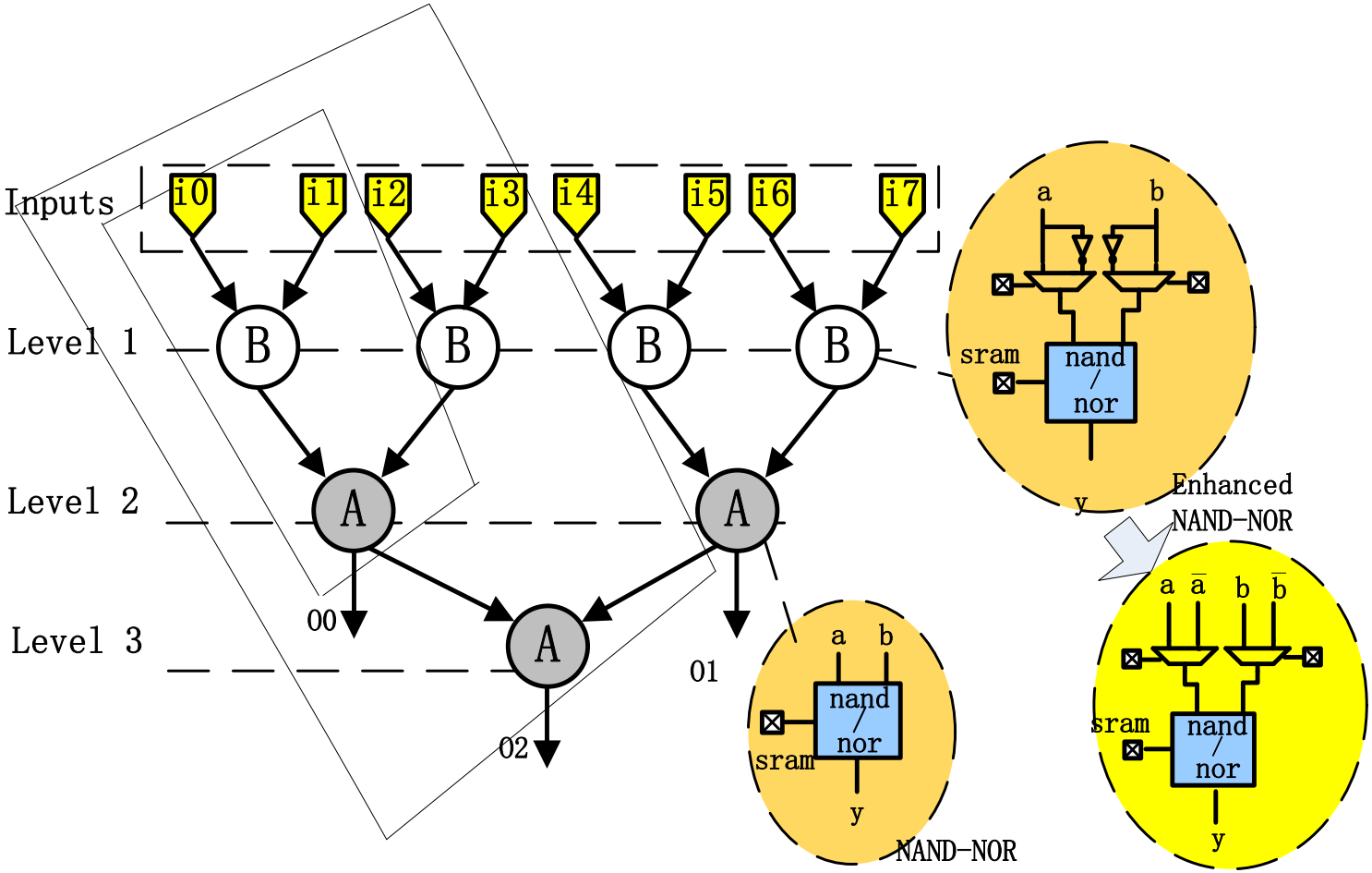
- The crossbars contribute to :
  - About 79% of the total cluster area
  - About 43% to 70% of the delay, depending on the selected path



The AIC cluster architecture adopted in the latest AIC paper

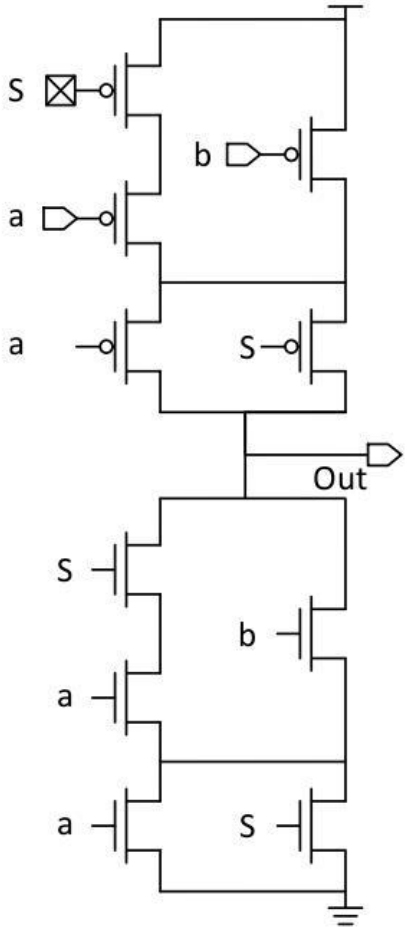
G. Zgheib, L. Yang, Z. Huang, D. Novo Bruna, H. Parandeh-Afshar, H. Yang, and P. Ienne. Revisiting And-Inverter Cones. In Proceedings of the 22nd ACM/SIGDA International Symposium on Field Programmable Gate Arrays, pages 45-54, Monterey,Calif., Feb. 2014.

NAND-NOR cone structure



A 3-level NAND-NOR with its different nodes

NAND-NOR element



Transistor-level implementation

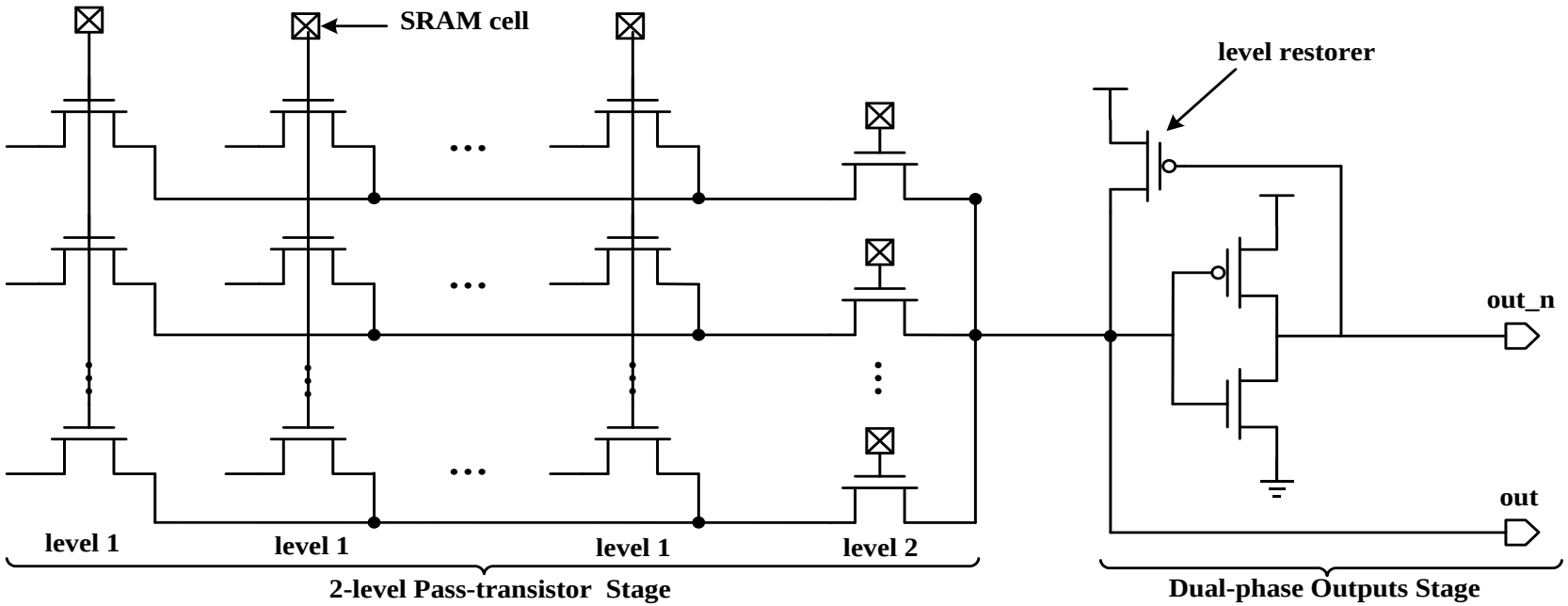
- The critical path traversed by the signal is reduced from 4 transistors to 2
- The total number of transistors is also reduced from 12 to 10

- Delay:
  - 14% - 46% improvement in average delay
  - 43% to 59% reduction in delay discrepancy

- Area:
  - 23% area reduction for a 6-level cone

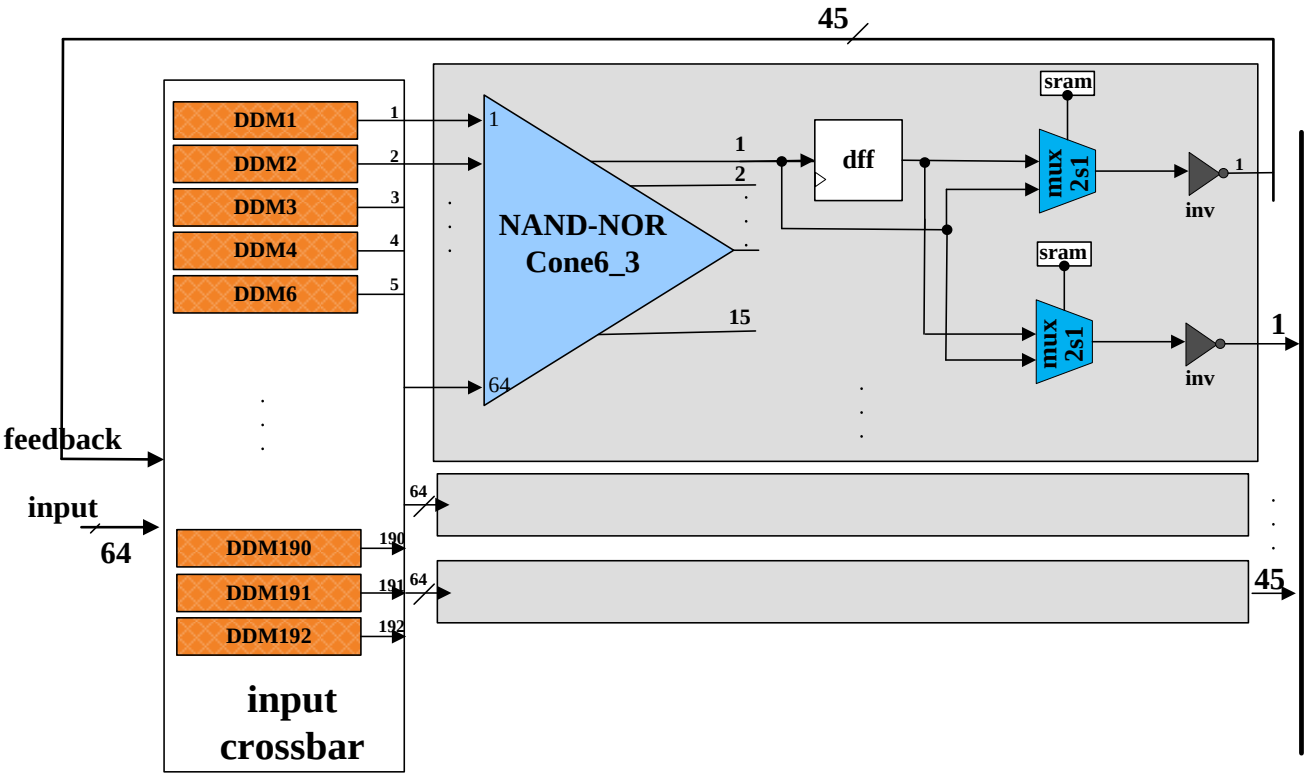
DDM input crossbar

- Delay-balanced Dual-phased Multiplexer (DDM)



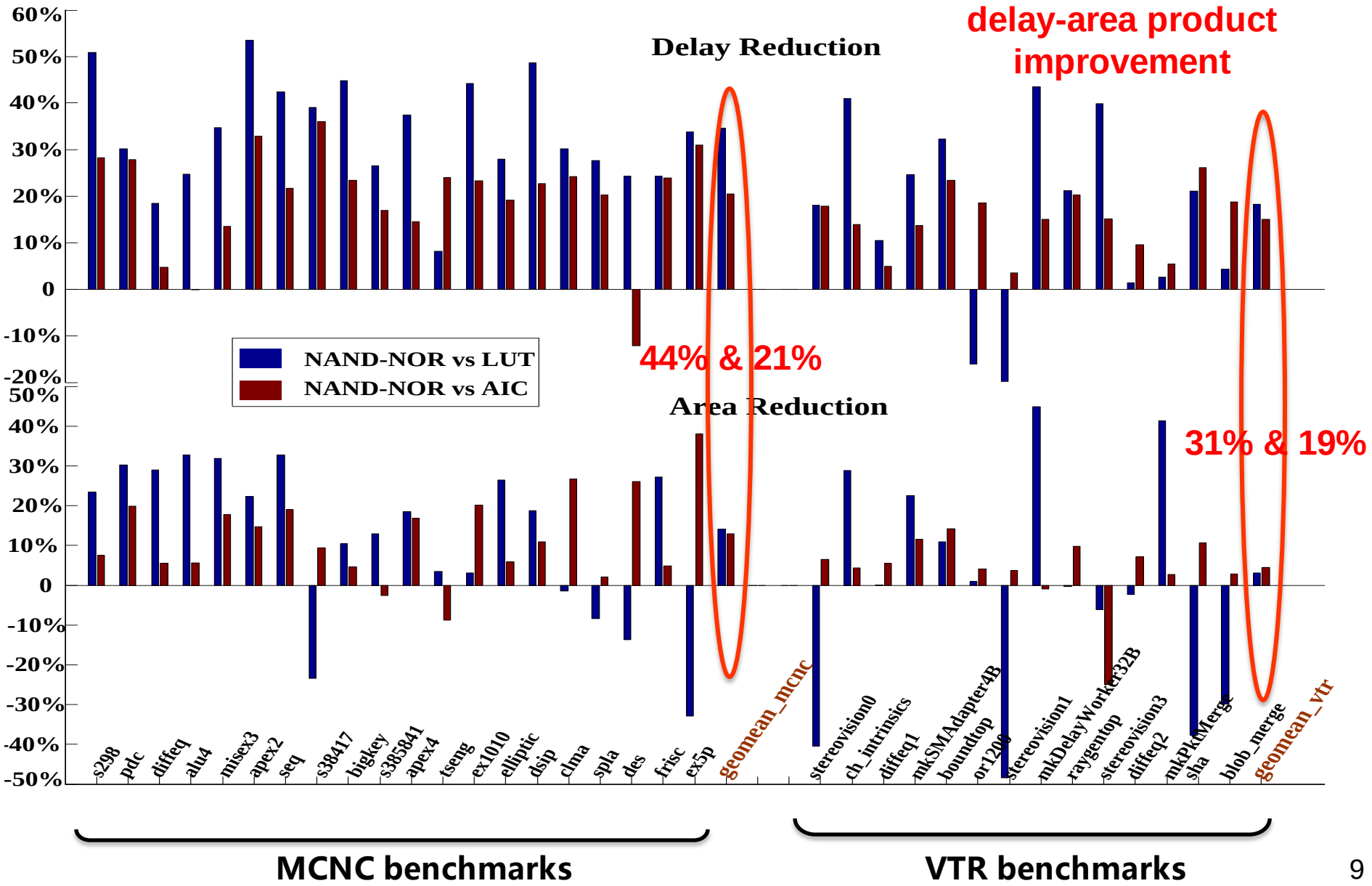
- Get both the output and its negation with relatively similar delays
- Removing the input inversions of the first level nodes: 28% area reduction for a 6-level cone
- The delay of the crossbar itself is also improved

Optimized logic cluster



- Removing the output crossbar
- Reducing the number of NAND-NOR Cone's outputs, thus removing middle crossbar
- Splitting between the feedback and direct output

Results


delay-area product improvement
Delay Reduction
NAND-NOR vs LUT
NAND-NOR vs AIC
44% & 21%
Area Reduction
31% & 19%
60%
50%
40%
30%
20%
10%
0
-10%
-20%
-30%
-40%
-50%
s298
pdc
diffeq
alu4
misex3
apex2
seq
s38417
bigkey
s385841
apex4
tseng
ex1010
elliptic
dsip
clma
spla
des
frisc
ex5p
geomean_mcnc
stereovision0
ch_intrinsics
diffeq1
mkSMAdapter4B
boundtop
or1200
stereovision1
mkDelayWorker32B
raygentop
stereovision3
diffeq2
mkPktMerge
sha
blob_merge
geomean_vtr
MCNC benchmarks
VTR benchmarks

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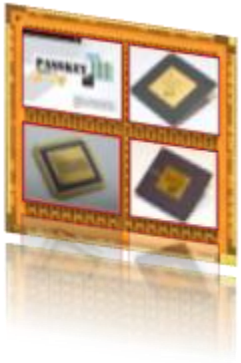

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