Just In Time Assembly of Accelerators

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Do you enjoy waiting for synthesis?
(Xilinx V7) Synthesis + Place & Route Time (mins)

Numbers of PEs
$S = \text{AVG}(dA, SA)$;

$S = \text{VMUL}(dA, dB, S)$;

$S = \text{RED}(dB, SB)$;
\[ S = \text{VMUL}(\text{AVG}(dA, SA), \text{RED}(dB, SB), S); \]
$$S=\text{VMUL}(\text{RED}(dA,SA),\text{AVG}(dB,SB),S);$$
\[ S = f_3(f_1 (dA, SA), f_2 (dB, SB), S); \]
\[ S = f_3( f_1 (dA, SA), f_2 (dB, SB), S); \]
Functor Template Library
int tmp = 0;
tmp = REDUCE ( VMUL (dataA, dataB, Size) );
int tmp = 0;
tmp = REDUCE (VMUL (dataA, dataB, Size));

User Application

Compile DSL

Build IR

Extract Patterns

Interpreter Call Generation

VAM_GET_Tile &PR1 U1
VAM_LOAD_Tile PR1 VMUL
VAM_GET_BRAM &BRAM1 dataA
VAM_GET_Tile &PR2 U2
VAM_GET_BRAM &BRAM2 dataB
VAM_LOAD_Tile PR2 REDUCE
VAM_GET_BRAM &BRAM3 tmp
VAM_DMA dataA BRAM1
VAM_DMA dataB BRAM2
VAM_ROUTE PR1 PR2
VAM_START PR1 PR2
VAM_DONE PR1 PR2
VAM_DMA BRAM3 tmp

Compiler

Portable Calls

BitStreams Repository

Bit-Streams

MicroBlaze (Application, OS + Interpreter*)

Tile Array

2 × 2 Tile Array on Xilinx Kintex 7

MicroBlaze (Application, OS + Interpreter*)

Tile Array

3 × 3 Tile Array on Xilinx Virtex 7

MicroBlaze (Application, OS + Interpreter*)

Tile Array

Tow 2 × 2 Tile Array on Xilinx Virtex 7

* Interpreters can be implemented in SW or in HW.
int tmp = 0;
tmp = REDUCE ( VMUL (dataA, dataB, Size ) );

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DFG Executable is Equivalent of Java Byte Code

Compiler

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BRAM Arrays

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Delite Compiler

DFG

Portable Calls

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tmp = REDUCE ( VMUL (dataA, dataB, Size ) );

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DFG Executable is Equivalent of Java Byte Code

Interpreter (aka JVM) allows DFG to execute on All platforms : Enables Portability

MicroBlaze
(Application, OS + Interpreter*)

Tile Array
PR
PR
PR
PR

BRAM Arrays

2 x 2 Tile Array on Xilinx Kintex 7

MicroBlaze
(Application, OS + Interpreter*)

Tile Array
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PR
PR
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MicroBlaze
(Application, OS + Interpreter*)

Tile Array
PR
PR
PR
PR

BRAM Arrays

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### Speedup

<table>
<thead>
<tr>
<th>Operation</th>
<th>MicroBlaze</th>
<th>HLS</th>
<th>JIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner Product</td>
<td>1x</td>
<td>10x</td>
<td>12x</td>
</tr>
<tr>
<td>3 Matrix Multiply</td>
<td>1x</td>
<td>8x</td>
<td>8x</td>
</tr>
<tr>
<td>Matrix × Vector</td>
<td>1x</td>
<td>24x</td>
<td>25x</td>
</tr>
<tr>
<td>Vector × Matrix</td>
<td>1x</td>
<td>26x</td>
<td>26x</td>
</tr>
<tr>
<td>Correlation</td>
<td>1x</td>
<td>5x</td>
<td>7x</td>
</tr>
</tbody>
</table>
Interesting:

✧ Size of overlay tile.
✧ Topology.
✧ Interconnect overhead.
✧ Programming model.
Thank you!
Come to see us in poster session!