Case for Design-Specific Machine Learning in Timing Closure of FPGA Designs

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Problem

• **Problem**: Timing Closure of FPGA designs hard. FPGA CAD tools difficult to control.

• **Opportunity**: Timing influenced by FPGA CAD parameters.

• **Solution**: Machine Learning + Cloud Computing.

• Design-Specific customisation of FPGA CAD parameter selection >> Generic selection
  — Not sufficient to simply use machine learning
  — Tailor the learning procedure to each design,
Requirement 4: Scale Out FPGA Tools in Cloud

- MS Cloud Tools
  - Run place-and-route and simulation tools on scalable resources
  - Speed up timing closure with parallel seeds
  - Must support determinism
  - Build caching shared amongst multiple users
  - Visual Studio integration
  - Partial reconfiguration
  - Static lock regions
“Speed up Timing Closure with parallel seeds”

Eric Chung (Microsoft) — “Agile Co-design for a Reconfigurable Datacenter”
FPGA 2016 Designer’s Day (yesterday!)
We do parallel seeds + machine learning!
High-Level View

• Idea:
  — Run multiple CAD tool instances in parallel
  — Build models of timing, devise strategies

• Machine Learning
  — Each CAD run == data point
  — Gather data

• Run machine-learning routines to revise models
Flow

- Organized as a series of “rounds”
  - Each “round” consists of multiple CAD “runs”

- Model used to generate candidate sets of CAD parameters
  - Refined/corrected after each “round”
  - Final round is a trivial seed exploration
Learning Approach

[Input] CAD Tool Parameters

[Output] Total -ve Slack

[Output] Better than baseline

Good

Bad

CAD Runs

$X_1, \ldots, X_p$

$X_1, \ldots, X_n$

$y_1, \ldots, y_p$

$f$
Learning Approach

[Input] CAD Tool Parameters

[Output] Total -ve Slack

[Output] Better than baseline

Trained per design or benchmark?
Results (aes)

best classification

![Classification Diagram]
Results (aes)

Random coin toss
Results (aes)
Conclusions

• Timing closure for FPGA designs is a challenge!

• FPGA CAD parameter selection offers a mechanism to deliver convergence — made possible by cheap cloud computing

• Design specific customisation AUC 0.7-0.8
  One-size fits all AUC 0.5-0.6 (random coin toss)

• Microsoft — We can give you a great discount!
## Ranked Features (aes)

<table>
<thead>
<tr>
<th>Rank</th>
<th>Design-Specific</th>
<th>Generic Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Optimize_Loc_Register_Placement_For_Timing</td>
<td>Remove_Redundant_Logic_Cells</td>
</tr>
<tr>
<td>2</td>
<td>Physical_Synthesis_Register_Retiming</td>
<td>Remove_Duplicate_Registers</td>
</tr>
<tr>
<td>4</td>
<td>Physical_Synthesis.Map_Lock_To_Memory_For_Area</td>
<td>Not_Gate_Push_Back</td>
</tr>
<tr>
<td>5</td>
<td>Auto_Rom_Recognition</td>
<td>Physical_Synthesis_Register_Duplication</td>
</tr>
<tr>
<td>6</td>
<td>Synth_Timing_Driven_Synthesis</td>
<td>Allow_Synch_Ctrl_Usg.</td>
</tr>
<tr>
<td>7</td>
<td>Extract_Vhd1_State_Machines</td>
<td>Auto_Resource_Share.</td>
</tr>
<tr>
<td>8</td>
<td>Dsp_Block_Balancing</td>
<td>Physical_Synthesis_Eff.</td>
</tr>
<tr>
<td>9</td>
<td>Fitter_Agressive_Routability_Optimiz.</td>
<td>Allow_Any_Ram_Size_For_Recognition</td>
</tr>
<tr>
<td>10</td>
<td>Cycloneii_Optimiz_Technique</td>
<td>Optimize_Timing</td>
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