FPRESSO
Enabling Express Transistor-Level Exploration of FPGA Architectures

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Architecture Exploration
Existing Tool: COFFE

Pros
• Parameterizable architecture
• Accurate delay/area measures

Cons
• Fixed structure
• Slow (several hours)

Objective

- Fast FPGA modeling
- Versatile architectures
- Accurate delay/area measures
- No user transistor expertise

Architecture description (e.g. VTR XML file) → Annotated architecture file (with delay/area values)
Objective

FPRESSO

Architecture description (e.g. VTR XML file) → FPRESSO → Annotated architecture file (with delay/area values)
<pb_type name="clb" num_pb="1" num_in="19" num_out="6">
  <pb_type name="ble" num_pb="6" num_in="6" num_out="2">
    <pb_type name="lut1" num_pb="1" num_in="4" num_out="1"/>
    <pb_type name="lut2" num_pb="1" num_in="4" num_out="1"/>
    <pb_type name="ff" num_pb="1" num_in="1" num_out="1" clock="clk"/>
    <mux name="combsqfdb" input="ff.Q lut2.out" output="ble.out[0]"/>
    <mux name="combsqfdb" input="ff.Q lut2.out" output="ble.out[1]"/>
    <direct name="lutina" input="ble.in[3:0]" output="lut1.in"/>
    <direct name="lutinb" input="ble.in[5:3]" output="lut2.in[3:1]"/>
    <direct name="lutinc" input="lut1.out" output="lut2.in[0]"/>
    <direct name="ffin" input="lut2.out" output="ff.d"/>
  </pb_type>
</pb_type>
<crossbar type="complete" name="inputxbar" input="clb.in ble.out[0]" output="ble.in"/>
<direct name="bleout" input="ble.out[1]" output="clb.out"/>
Interface

Architecture description → FPRESSO → Annotated architecture file
Complete Flow

Architecture description

Library Generation

Main Flow

Use existing standard cell tools?

Annotated architecture file
Main Flow

Library

Architecture description

Verilog generator

Design Compiler

Timing/area extractor

Architecture file generator

Annotated architecture file
Library Generation

Process models

SPICE netlist generator

Modified COFFE
Library Generation

Process models

SPICE netlist generator

Modified COFFE

K-LUT

Input crossbar

BLE_0

BLE_1

BLE_{n+1}

FF
Library Generation

Process models

SPICE netlist generator

Modified COFFE
Library Generation

SPICE netlist generator

Modified COFFE

Process models

Netlist_1, Netlist_2, Netlist_3, Netlist_4, Netlist_5, ...

L_1, L_2, L_3, L_4, L_5, ...

Input crossbar

BLE_{i+1}
Library Generation

Process models → Modified COFFE → SPICE netlist generator

SPICE netlists with different transistor sizes

K-LUT

2LUT₁, 2LUT₂, 2LUT₃, 2LUT₄, ...
3LUT₁, 3LUT₂, 3LUT₃, 3LUT₄, ...
...

Mux

Mux₁, Mux₂, Mux₃, Mux₄, ...
Mux₂x2₁, Mux₂x2₂, Mux₂x2₃, Mux₂x2₄, ...
...

2-Level Mux

Mux₃x3₁, Mux₃x3₂, Mux₃x3₃, Mux₃x3₄, ...
...

SPICE netlist generator

Modified COFFE
Library Generation

Offline generation

- Process models
- Modified COFFE
- SPICE netlists with different transistor sizes
- Components characterization
- Cadence Liberate
- Library file
Complete Flow

- **Library Generation**
  - Library

- **Main Flow**
  - Architecture description
  - Annotated architecture file
Library Generation

SPICE netlist generator
Modified COFFE

SPICE netlists with different transistor sizes

Component Characterization
Cadence Liberate

Complex functionality
Large number of variables

Library file
LUT Characterization

3-LUT $\rightarrow$ 11 variables

6-LUT $\rightarrow$ 70 variables
Main Flow

Architectural description

Library

- Verilog generator
- Timing/area extractor
- Architecture file generator

Design Compiler

Annotated architecture file
Combinational Loops
FPRESSO

Architecture description

Annotated architecture file

Library

Library Generation

Main Flow

Library
FPRESSO vs. COFFEE

Parameters
- K: Number of LUT inputs
- N: Number of BLEs
- I: Number of cluster inputs
- Complete input crossbar
- Delay optimization

Differences
- No wire load models
- Estimated switch block capacitance
Results

CLB’s IO path

Feedback path

Area

-20% -10% 0% 10% 20%

Delay

-40% -20% 0% 20% 40%

Area

-20% -10% 0% 10% 20%

Delay

-40% -20% 0% 20% 40%

K4_N6_119
K4_N6_130
K4_N6_143
K5_N6_119
K5_N6_130
K5_N6_143
K5_N8_128
K5_N8_141
K6_N6_119
K6_N6_130
K6_N6_143
K6_N8_128
K6_N8_143
K6_N10_126
Fidelity of FPRESSO w.r.t. COFFE
Area-Delay Pareto Front

Fixed architecture: K = 5, N = 6 and I = 30
<pb_type name="clb" num_pb="1" num_in="19" num_out="6">
   <pb_type name="ble" num_pb="6" num_in="6" num_out="2">
      <pb_type name="lut1" num_pb="1" num_in="4" num_out="1"/>
      <pb_type name="lut2" num_pb="1" num_in="4" num_out="1"/>
      <pb_type name="ff" num_pb="1" num_in="1" num_out="1" clock="clk"/>
      <mux name="combseqfdbc" input="ff.Q lut2.out" output="ble.ble[0]"/>
      <mux name="combseqout" input="ff.Q lut2.out" output="ble.ble[1]"/>
      <direct name="lutinA" input="ble.in[3:0]" output="lut1.in"/>
      <direct name="lutinB" input="ble.in[5:3]" output="lut2.in[3:1]"/>
      <direct name="lutinC" input="lut1.out" output="lut2.in[0]"/>
      <direct name="ffin" input="lut2.out" output="ff.D"/>
   </pb_type>
   <crossbar type="complete" name="inputxbar" input="clb.in ble.out[0]" output="ble.in"/>
   <direct name="bleout" input="ble.out[1]" output="clb.out"/>
</pb_type>
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